Efficient Built In Self Repair Strategy for Embedded SRAM with selectable redundancy

*GUDURU MALLIKARJUNA **Dr. P. V.N.REDDY

* (ECE, GPCET, Kurnool. E-Mailid:mallikarjuna3806@gmail.com)

** (Professor, Dept. of ECE, GPCET, Kurnool. E-Mail id: pvnreddy_alfa@rediffmail.com)

***Abstract*— Built-in self-test (BIST) refers to those testing techniques where additional hardware is added to a design so that testing is accomplished without the aid of external hardware. Usually, a pseudo-random generator is used to apply test vectors to the circuit under test and a data compactor is used to produce a signature.**

To increase the reliability and yield of embedded memories, many redundancy mechanisms have been proposed. All the redundancy mechanisms bring penalty of area and complexity to embedded memories design. Considered that compiler is used to configure SRAM for different needs, the BISR had better bring no change to other modules in SRAM. To solve the problem, a new redundancy scheme is proposed in this paper. Some normal words in embedded memories can be selected as redundancy instead of adding spare words, spare rows, spare columns or spare blocks.

Built-In Self-Repair (BISR) with Redundancy is an effective yield-enhancement strategy for embedded memories. This paper proposes an efficient BISR strategy which consists of a Built-In Self-Test (BIST) module, a Built-In Address-Analysis (BIAA) module and a Multiplexer (MUX) module. The BISR is designed flexible that it can provide four operation modes to SRAM users. Each fault address can be saved only once is the feature of the proposed BISR strategy. In BIAA module, fault addresses and redundant ones form a one-to-one mapping to achieve a high repair speed. Besides, instead of adding spare words, rows, columns or blocks in the SRAMs, users can select normal words as redundancy.

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1. Introduction

Nowadays, the area occupied by embedded memories in System-on-Chip (SoC) is over 90%, and expected to rise up to 94% by 2014. Thus, the performance and yield of embedded memories will dominate that of SoCs. However, memory fabrication yield is limited largely by random defects, random oxide pinholes, random leakage defects, gross processing and assembly faults, specific processing faults, misalignments, gross photo defects and other faults and defects.

To increase the reliability and yield of embedded memories, many redundancy mechanisms have been proposed. In both redundant rows and columns are incorporated into the memory array. In spare words, rows, and columns are added into the word-oriented memory cores as redundancy. All these redundancy mechanisms bring penalty of area and complexity to embedded memories design. Considered that compiler is used to configure SRAM for different needs, the BISR had better bring no change to other modules in SRAM. To solve the problem, a new redundancy scheme is proposed in this paper. Some normal words in embedded memories can be selected as redundancy instead of adding spare words, spare rows, spare columns or spare blocks.

Memory test is necessary before using redundancy to repair.

Design for test (DFT) techniques proposed in 1970 improves the testability by including the testability by including additional circuitry. The controlled

Through a BIST circuitry is more time-saving and efficient compared to that controlled by the external tester (ATE). However, memory BIST does not address the loss of parts due to manufacturing defects but only the screening aspects of the manufactured parts. BISR techniques aim at testing embedded memories, saving the fault addresses and replacing them with redundancy. In, the authors proposed a new memory BISR strategy applying two serial redundancy analysis (RA) stages. Presents an efficient repair algorithm for embedded memory with multiple redundancies and a BISR circuit using the proposed algorithm. All the previous BISR techniques can repair memories, but they didn't tell us how to avoid storing fault address more than once. This paper proposes an efficient BISR strategy which can store each fault address only once.

The rest of this paper is organized as follows. Section II outlines SRAM fault models, test algorithms and BIST design. Section III introduces the proposed BISR strategy. We present the details of the proposed BISR strategy including the architectures, procedures and the features. In section IV, the experimental results are reported. Finally, Section V concludes this paper.

2.EXISTING SYSTEM

Previously the memory devices were tested and repaired using a software technique. In this software technique there was the use of redundancy logic. The disadvantage of redundancy logic is the usage of extra buffers for storing the faulty addresses, data and also flags..

3. PROPOSED SYSTEM

According to the paper the proposed architecture uses the Selectable Redundancy for repairing a memory. This can be done by having redundancy words and mapping the faulty addresses to these redundancy addresses.

Memory testing is a more and more important issue

- RAMs are key components for electronic systems
- Memories represent about 30% of the semiconductor market
- Embedded memories are dominating the chip yield.

Memory testing is more and more difficult

- Growing density, capacity, and speed
- Emerging new architectures and technologies
- Embedded memories: access, diagnostics & repair, heterogeneity, custom design, power & noise, scheduling, compression, etc.

Cost drives the need for more efficient test methodologies

- IFA, fault modeling and simulation, test algorithm development and evaluation, diagnostics, DFT, BIST, BIRA, BISR, etc.

Test automation is required

- Failure analysis, fault simulation, ATG, and diagnostics
- BIST/BIRA/BISR generation

Embedded memory testing is increasingly difficult

- High bandwidth (speed and I/O data width)
- Heterogeneity and plurality
- Isolation (accessibility)
- AC test, diagnostics, and repair

BIST is considered the best solution. Because, for Embedded memories accessibility of Pins is not sufficient for testing outside the chip.

4. Proposed Algorithm

The details of fault models can be referred in. they are the foundations of the memory test. An efficient and economical memory test should provide the best fault coverage in the shortest test time. BIST is used to test memories in the paper and its precision is guaranteed by test algorithms. March tests have the advantage of short test time but good fault coverage. There are many March tests such as March C, March C-, March C+, March 3 and so on. TABLE 1 compares the test length, complexity and fault coverage of them. 'n' stands for the capacity of SRAM.

TABLE 1: COPARISON OF DIFFERENT MARCH TESTS

Algorithms	Test length	Complexity	Fault coverage
March C	11n	O(n)	AF,SAF,TF,CFin CFid, and CFst.
March C-	10n	O(n)	AF,SAF,TF,CFin CFid, and CFst
March C+	14n	O(n)	AF,SAF,TF,CFin CFid, and CFst
March 3	10n	O(n)	AF,SAF,SOF, and TF

As shown in TABLE 1, March C- has better fault coverage than March 3 and shorter test time than March C and March C+. So March C- has been chosen as BIST algorithm in this paper.

Its algorithm steps are as follows:

Up	-write 0
Up	-read 0, write 1
Up	-read 1, write 0
Down	-read 0, write 1
Down	-read 1, write 0
Down	-read 0

In above steps, "up" represents executing SRAM addresses in ascending order while "down" in descending order.

The BIST module in the paper refers to the MBISR design of mentor Graphics; it mainly consists of a BIST controller, a test vector generator and a comparator. It can indicate when memory test is done and weather there is fault in memory.

5. Proposed BISR Strategy

A Redundancy Architecture

The proposed SRAM BISR strategy is flexible. The SRAM users can decide whether to use it by setting a signal. So the redundancy of the SRAM is designed to be selectable. In another word, some normal words in SRAM can be selected as redundancy if the SRAM needs to repair itself. We call these words Normal-Redundant words to distinguish them from the real normal ones. We take 64 x 4 SRAM for example, as shown in figure 1. There are 60 normal words and 4 Normal-Redundant words. When the BISR is used, the Normal-Redundant words are accessed as normal ones. Otherwise, the Normal-Redundant words can only be accessed when there are faults in normal words. In this case, the SRAM can only offer capacity of 60 words to users. This should be referred in SRAM manual in detail.

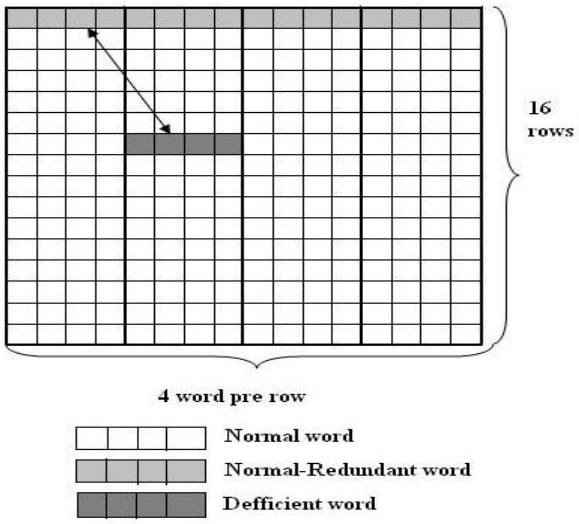

figure 1: Architecture of Redundancy in SRAM

This kind of selectable redundancy architecture can save area and increase efficiency. After BISR is applied, other modules in SRAM can remain unchanged. Thus the selectable redundancy won't bring any problem to SRAM compiler.

B. Overall BISR Architecture

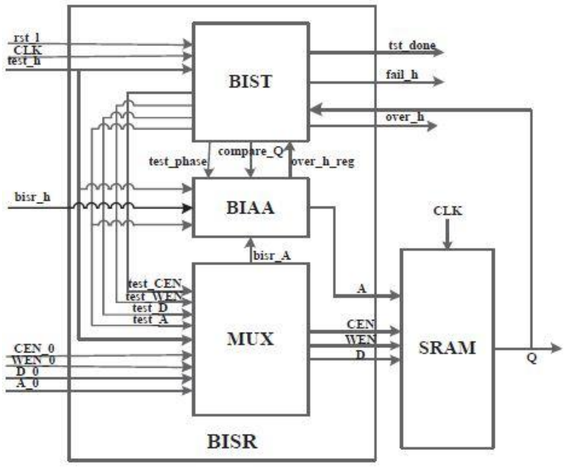

Figure 2: proposed BISR Architecture

The Architecture o the proposed BISR strategy is shown in figure 2. It consists of three parts: BIST module, BIAA module and MUX module. We call the SRAM with BISR a system. The BIST module uses march C- to test the addresses of the normal words in SRAM. It detects SRAM failures with a comparator that compares actual memory data with expected data. If there is a failure (Compare_Q=1),the current address is considered as a faulty address. The BIAA module can store faulty addresses in a memory named Fault_A_Mem. There is a counter in BIAA that counts the number of faulty addresses. When BISR is used (bisr_h=1), the faulty addresses can be replaced with redundant addresses to repair the SRAM. The inputs of SRAM in different operation modes are controlled by the MUX module. In test mode (bist_h=1), the inputs of SRAM are generated in BISR while they are equal to system inputs in access mode (bist_h=0).

C. BISR Proedure

Figure 3shows the Proposed BISR block diagram. The BISR starts by resetting the system (rst_h=1). After that if the system work in test mode, it goes into TEST phase. During this phase, the BIST module and BIAA module work in parallel. The BIST use March C- to test the normal addresses of SRAM. As long as any fault is detected by the BIST module, the faulty address will be sent to the BIAA module. Then the BIAA module checks whether the faulty address has been already stored in Fault-A-Mem. If the faulty address has not been stored, the BIAA stores it and the faulty address counter adds 1. Otherwise, the faulty address can be ignored. When the test is completed, there will be two conditions. If there is no fault or there are too many faults that overflow the redundancy capacity, BISR goes into COMPLETE phase. If there are faults in SRAM but without overflows, the system goes into REPAIR&TEST phase. The BIAA module replaces the faulty addresses stored in Fault-A-Mem with redundant ones and the BIST module tests the SRAM again. There will be two results: repair fail or repair pass. By using the BISR, the users can pick out the SRAMs that can be repaired with redundancy or the ones with no fault.

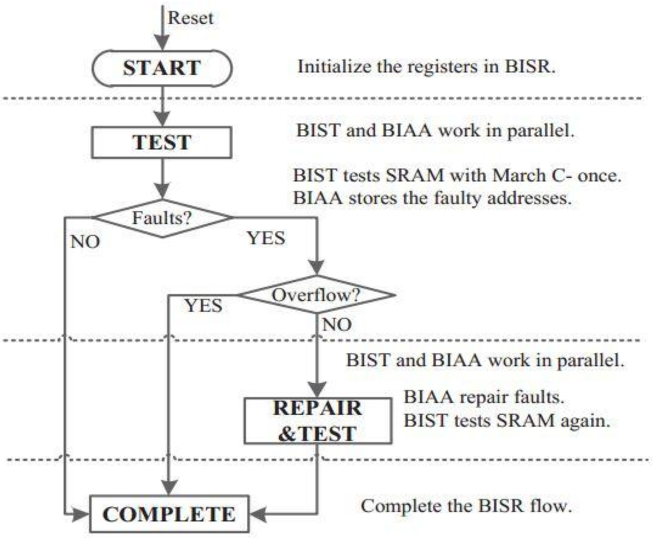
Reset
START
Initialize the registers in BISR.
TEST
BIST and BIAA work in parallel.
BIST tests SRAM with March C- once.
BIAA stores the faulty addresses.
Faults?
NO
YES
Overflow?
YES
NO
BIST and BIAA work in parallel.
REPAIR &TEST
BIAA repair faults.
BIST tests SRAM again.
COMPLETE
Complete the BISR flow.

Figure 3: Block Diagram of BISR

D. Features of the BISR

Firstly, the BISR strategy is flexible. TABLE II lists the operation modes of SRAM. In access mode, SRAM users can decide whether the BISR is used base on their needs. If the BISR is needed, the Normal-Redundant words will be taken as redundancy to repair fault. If not, they can be accessed as normal words. Secondly, the BISR strategy is efficient. On one hand, the efficiency reflects on the selectable redundancy which is described as flexible above. No matter the BISR is applied or not, the Normal-Redundant words are used in the SRAM. It saves area and has high utilization. On the other hand, each fault address can be stored only once into Fault-A-Mem. As said before, March C- has 6 steps. In another word, the addresses will be read 5 times in one test.

Modes	Repair selection	Operation
Test mode (test_h=1)	Default repair (bisr_h=1)	Access normal words. Repair faults and test.
	Don’t repair (bisr_h=0)	Access normal words. Test only.
Access mode (test_h=0)	Repair (bisr_h=1)	Access normal words. Repair faults and w/r SRAM
	Don’t repair (bisr_h=0)	Access normal redundant and normal words. w/r SRAM only.

Some faulty addresses can be detected in more than one step. Take Stuck- at-0 fault for example, it can be detected in both 3rd and 5th steps. But the fault address shouldn't be stored twice. So we propose an efficient method to solve the problem in BIAA module. Figure 4 shows the flows of storing fault addresses. BIST detects whether the current address is faulty. If it is, BIAA checks whether the Fault-A-Mem overflows. If not, the current fault address should be compared with those already stored in Fault-A-Mem. Only if the faulty address isn't equal to any address in Fault-A-Mem, it can be stored. To simply the comparison, write a redundant address into Fault-A-Mem as background. In this case, the fault address can be compared

With all the data stored in fault-A-Mem no matter how many fault addresses have been stored.

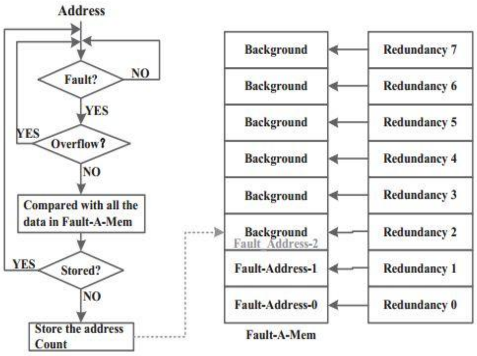

Figure 4: flows of storing fault address

At last, the BISR strategy is high-speed. As shown in figure 4, once a fault address is stored in Fault-A-Mem, it points to a certain redundant address. The fault addresses and redundant ones from a one-to-one mapping. Using this method, the BISR can quickly get the corresponding redundant address to replace the faulty one.

6. Experimental results

The proposed BISR was designed at RT level and it was synthesized to gate-level using Synopsys DC compiler. We use cadence SOC Encounter to complete physical design of a 4K x 32 SRAM with BISR. The post simulation results show that the frequency of SRAM with BISR is at least 150MHz. the SRAM was implemented based on a 55nm CMOS process. The 32 addresses from H'FFF were selected as Normal-Redundant addresses. To verify the function of BISR, a Stuck-at-0 fault was set in the SRAM. Figure 5 shows the layout view of the SRAM with BISR circuitry. BISR brings about 20% area penetrates.

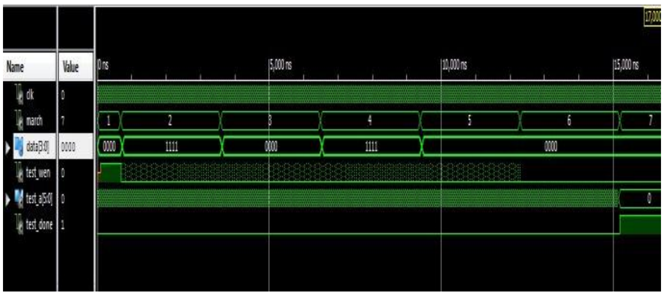

Figure 5: BIST Simulation

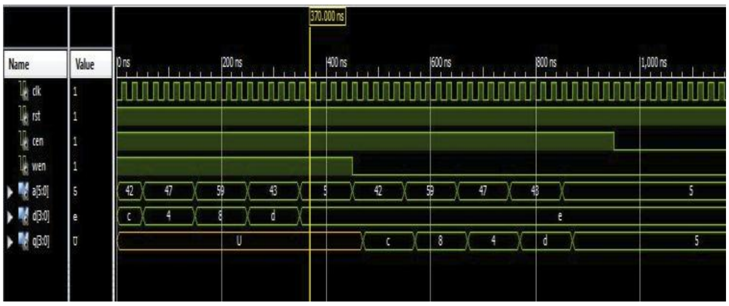

Figure 6: SRAM simulation

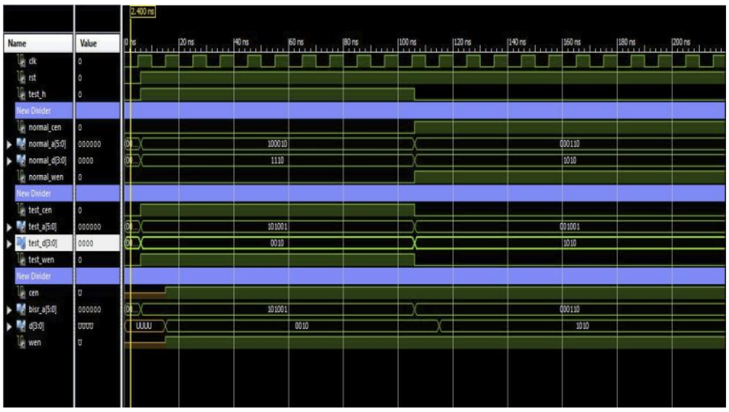

Figure 7: Mux Simulation

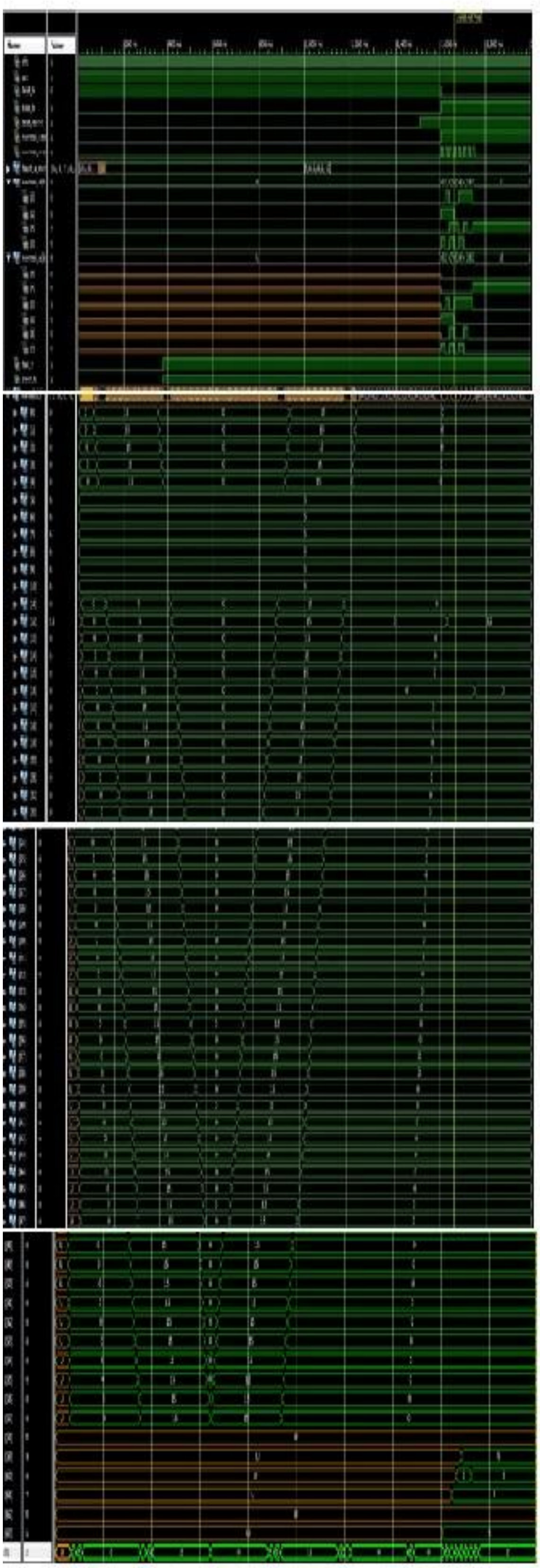

Figure 8: simulation of top BISR module

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BIBLIOGRAPHY

Dr. P. VEERA NARAYANA REDDY received the B.Tech degree in Electronics and Communication Engineering from K.S.R.M College of Engineering, Kadapa, S.V.University, Tirupathi, A.P. in 1986. and received his M. Tech Post Graduate in Digital System and Computer Electronics from JNTU College of Engineering , Anatapur JNT University in 2003 and He got Ph.D in Digital Image Processing from JNTU Kakinada in 2013.

He has Life member ship in I.S.T.E.

He published 17 technical papers in various International journal, International and National conferences.

Currently he is working as Professor & HOD of ECE Department in G.PULLAIAH COLLEGE OF ENGG & TECH KURNOOL, JNTU Anantapur, A.P. His current research interests include Digital Image Processing and Analog & digital Communications.

Ms. GUDURU MALLIKARJUNA received the B.Tech degree in Electronics and Communication Engineering from Intell Engineering College,Anantapur, JNTU Anantapur, A.P in 2011.

Currently she is pursuing G.PULLAIAH COLLEGE OF ENGG & TECH KURNOOL, JNTU Anantapur, A.P.

His current research interests include VLSI and Low power CMOS DESIGN.