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A Review on VHDL Implementation for Adaptive Finite Impulse Response filter and its novel applications using Systolic Architecture

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Abstract-The evolution of computer and Internet has brought demand for powerful and high speed data processing. In such complex environment, the conventional methods of performing matrix multiplications are not suitable to obtain the perfect solution. To handle above addressed issue, parallel computing is proposed as a solution to the contradiction. The DLMS adaptive algorithm minimizes approximately the mean square error by recursively altering the weight vector at each sampling instance. This project demonstrates an effective design for adaptive filter using Systolic architecture, synthesized and simulated on Xilinx ISE 12.1 Project navigator tool in very high speed integrated circuit hardware description language (VHDL) using Systolic Architecture on Reconfigurable Systems (RS) like Field Programmable Gate Arrays (FPGAs). Here, the systolic architecture increases the computing speed by combining the concept of parallel processing and pipelining into a single concept.

Keywords *—Algorithms, Sampling, Systolic Architecture, parallel processing, pipelining.*

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I. INTRODUCTION

In computer architecture, a systolic architecture is a pipelined network arrangement of Processing Elements (PEs) called cells. It is a specialized form of parallel computing, where cells compute the data which is coming as input and store them independently. Systolic architecture represent a network a processing element (PEs) that rhythmically compute and pass data through the stem the PEs regularly pump data in an out such that regular flow of data is maintained, as a result systolic array feature modularity and regularity which are property for VLSI design the systolic array may be used as a coprocessor in combination of host computer pass through PEs and the final result is return to host computer (See fig 1).

In order to achieve the high speed and low power demand in ASP applications, parallel array multipliers are widely used. In DSP applications, most of the power is consumed by the multipliers. Hence, low power multipliers must be designed in order to reduce the power dissipation

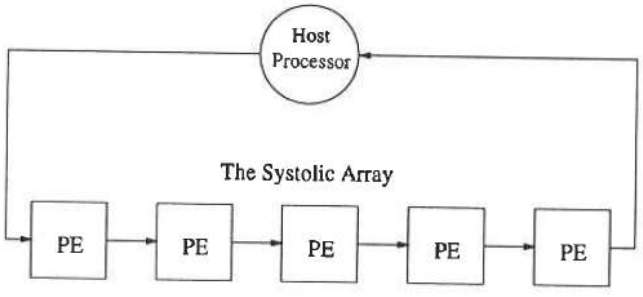

Figure 1.Basic Principle of systolic system

$$y(n) = \mathbf{w}^T(n)\mathbf{x}(n)$$
$$e(n) = d(n) - y(n)$$
$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu e(n)\mathbf{x}(n)$$

The LMS adaptive algorithm minimizes approximately the mean-square error by recursively altering the weight vector at each sampling instance. Thus, an adaptive FIR digital filter driven by the LMS algorithm can be described in vector form as

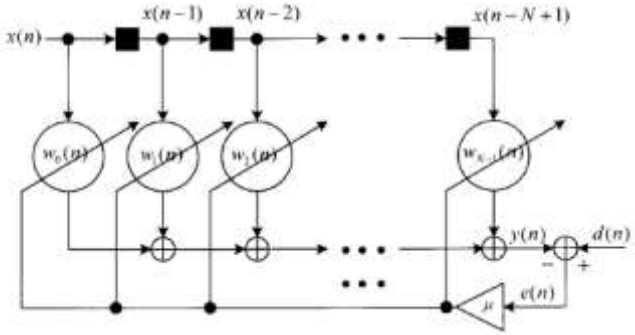

Figure 2. Block diagram of an adaptive FIR digital filter driven by LMS algorithm

Where N is the length of an FIR digital filter and denotes the transpose operator. The block diagram of the LMS adaptive FIR digital filter is depicted in Fig. 2, where the symbol denotes the unit delay element. The coefficient update using the DLMS algorithm [5] of an -tap adaptive FIR digital filter is represented by the following equation and where D is the delay value in weight adaptation.

II. LITERATURE REVIEW ONADAPTIVE FINITE IMPULSE RESPONSE FILTERDESIGN

One of the important implementation of the Systolic array architecture given by Bairu K. Saptalakar, Deepak kale, Mahesh Rachannavar, Pavankumar M. K, these implementation involve systolic array multiplier which was designed for 4 bits using structural and behavioral styles and was implemented, tested on the Spartan-3 FPGA board. In structural modeling, multiplier is divided into 3 sections i.e. upper, middle and lower sections. Where, all the three sections operate on the data simultaneously. Full adder and AND gates were used as the basic building blocks of the multiplier. Each section has 4 full adders and associated AND gates. The behavioral description was written and implemented based on the behavior of the Systolic Array multiplier. A timing analysis tool was then applied to the object module to determine maximum operating speed. Thus the design of 4 bit Systolic Array Multiplier in this design was optimized using structural style compared with behavioral style [1].

Another important implementation of low power systolic base adaptive filter is suggested by Purushothaman A, Dr. C. Vijaykumar. Design uses systolic architecture for RLS using FPGA technology with clock getting and used systolic architecture instead of adders, subtracters and multipliers Systolic arrays speed up the processing due to the parallel calculation, but have the major difficulty that the circuit scale becomes extremely large if the number of elements was large. The clock gating technique was extensively used in the design of low-power circuit .It involves dynamically shutting off the clock to portions of a design that are idle or are not performing usefulcomputation. The result of implementing the RLS algorithm in FPGA using systolic arrays adopting the reusable configuration and clock gating was use for the internal cells design. For the cases of two and four antenna elements, the required number of sampling data processing clock cycles was 20, which indicates that the weights are updated using a very small number of clock cycles. The total numbers of clock cycles required before convergence for the two and four antenna element cases were 320 and 540, respectively [2].

Another important implementation of systolic array architecture for matrix multiplication by MahendraVucha, ArvindRajawat. Design uses Systolic Array architecture for Matrix multiplication algorithm .algorithm can be implemented in two methods 1. Conventional method (with-out Pipeline and Parallel Processing) 2. Systolic

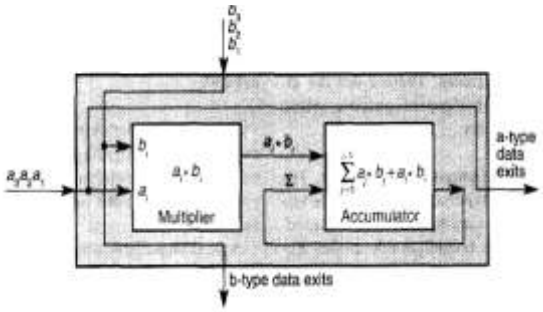

Figure 3.PE of systolic Architecture

Architecture (Pipeline and Parallel Processing). In this design the PE was replaced with multiplication and Accumulation (MAC) to enhance the speed and reduce the complexity of Systolic Architecture. The implementation of Matrix Multiplication was done in both methods i.e. Conventional and Systolic Architecture on FPGA. The RTL code was written in Verilog HDL, verification of logic and simulation was done by Modelsim XE 6.4b. The simulation results have given that, the Systolic architecture implementation requires less number of clock cycles than Conventional method. Where input and output matricesA3×3, B3×3 and C3×3 respectively, where the matrix elements were 4 bit each. The parallel processing and pipelining was introduced into the proposed systolic architecture to enhance the speed and reduce the complexity of the Matrix Multiplier [3].

Another important implementation by Feifei Dong, Sihan Zhang and Cheng Chen, improved design and analyze of parallel matrix multiplication on systolic array matrix. This design deals with the problem and demonstrates an improved algorithm for the traditional Parallel Matrix multiplication on Systolic Array, which was widely applied in the architecture of Central Processing Unit (CPU). It also analyzes and proves merits of the improvement. And introduces an improved Systolic matrix vector based algorithm to maximize utilization of parallel processors [6].

Another important implementation by Hanan Herzberg and RazielHaimi-Cohen, A systolic array realization of an LMS adaptive filter and the effects of delayed adaptation. This design uses systolic array for adaptive filter. The filter was based on the least mean square (LMS) algorithm but due to the problems in implementation of the systolic array a modified algorithm, a special case of the delayed LMS (DLMS) was use. The DLMS algorithm introduces a delay in the updating of the filter coefficients. The convergence and steady state behavior of the systolic array were analyzed. It is shown that the performance of the systolic array was similar to that of a conventional LMS implementation [7].

Another important implementation by M. D. Meyer and D. P. Agrawal, A high sampling rate delayed LMS filter architecture. This implementation show the problem of

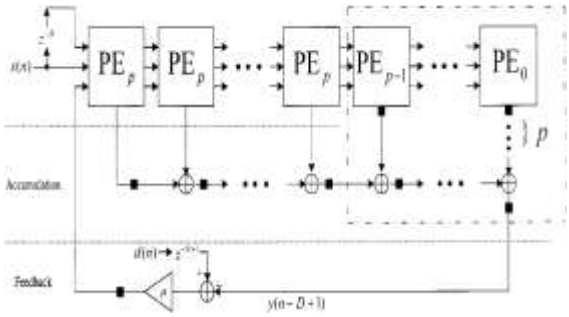

Figure 4.Systolic architecture with Cascaded Systolic-Tree PEs

Implementing a high sampling rate transversal form adaptive filter was investigated. A highly pipelined systolic-type alternative to the conventional LMS adaptive filter was presented. The resulting adaptive filter structure can accommodate very high sampling rates, which were independent of the filter order. The performance of the system was analyzed in terms of computational speedup and maximum sampling rate, and the effect of adaptation delay on algorithm convergence was addressed. A modular and highly parallel alternative to the conventional LMS algorithm had been presented. The pipelined filter structure, which implements a parallel version of the DLMS algorithm, uses multiple identical processing modules to achieve a computational speed up proportional to the order of the filter [8].

Another important implementation by R. D. Poltmann, Conversion of the delayed LMS algorithm into the LMS algorithm .The design shows the way how the delayed LMS (DLMS) algorithm can be transformed into the standard LMS algorithm at only slightly increased computational expense [10].

Another important implementation by Lan-Da Van AND Wu-ShiungFeng, An efficient systolic architecture for the DLMS adaptive filter and its applications. This design uses an efficient systolic architecture for the delay least-mean-square (DLMS) adaptive finite impulse response (FIR). Digital filter based on a new tree-systolic processing element (PE) and an optimized tree-level rule. It provides comprehensive comparison results for different -tap adaptive FIR filter structure and verify our systolic-array architecture of adaptive equalization and system identification applications [11].

Another important implementation by Fábio Fabian Daitx, Vagner S. Rosa, Eduardo Costa, Paulo Flores, SérgioBampi, VHDL generation of optimized FIR filters. In this design a near optimum algorithm for constant coefficient FIR filters was used. This algorithm uses general coefficient representation for the optimal sharing of partial products in Multiple Constants Multiplications (MCM). The software implementation was developed in C language and produces VHDL code for the optimized FIR filter from a coefficient specification file. The developed software was applied to several FIR filters and compared to MATLAB Filter Design & Analysis (FDA). The FDA toolbox includes a feature to generate optimized VHDL code from the generated coefficients and was used to compare to the developed software [12].

Another important implementation by Pramod K. Meher and Megha Maheshwari, A high-speed FIR adaptive filter architecture using a modified delayed LMS algorithm. This design uses a modified delayed least means square (DLMS) adaptive algorithm to achieve lower adaptation-delay and an efficient pipelined architecture for the implementation of adaptive filter. Design shows that the DLMS adaptive filter can be implemented by a pipelined inner-product computation unit for calculation of feedback error, and a pipelined weight-update unit consisting of N parallel multiplies accumulators for filter order N. And suggested a modified DLMS adaptive algorithm to achieve less adaptation-delay compared with the conventional DLMS algorithm [13].

Another important implementation by K. R. Santha and V Vaidehi, A new pipelined architecture for the DLMS algorithm. This paper presented a design of systolic array architecture for the 1-dimensional Finite Impulse Response adaptive filter. The design was based on the Delayed Least Mean Squares algorithm (DLMS). Performance of the design was analyzed in terms of speed up, adaptation delay and throughput. The different N-tap 1 -D adaptive filters were analyzed and it shows that the proposed scheme was superior in terms of adaptation delay, speed and throughput without the need for additional hardware [14].

Another important implementation by Lan-Da Van and Wu-ShiungFeng, efficient systolic architectures for l-D and 2-D DLMS adaptive digital. Two efficient Nth tap 1-D and window size N x N 2-D systolic adaptive digital filters utilizing the tree-systolic PE had presented. Under considering maximum number of tap-connections of the feedback error signal, the practical rule to decide the optimized tree level without sacrificing the systolic characteristics was provided. At last verify I-D and 2-D efficient systolic architectures via applications of adaptive equalizer and image restoration [15].

Another important implementation by S. Ramanathan and V. Visvanathan, A Systolic Architecture for LMS Adaptive Filtering with Minimal Adaptation Delay. This design presented a systolic architecture with minimal adaptation delay and input/output latency, thereby improving the convergence behavior to near that of the original LMS algorithm. The architecture was synthesized by using a number of function preserving transformations on the signal flow graph representation of the delayed LMS algorithm. With the use of carry-save arithmetic the systolic folded pipelined architecture can support very high sampling rates elimited only by the delay of a full adder [16].

Another important implementation by Basant K. Mohanty, Promod K. Meher, delayed block LMS algorithm and concurrent architecture for high-speed implementation of adaptive FIR filter. In this design the DBLMS algorithm which takes a block of L input samples and yields a block of L outputs in every training cycle was used. The simulation result shows that the performance of DBLMS algorithm was equivalent to that of the DLMS algorithm. However, the DBLMS algorithm offers L fold higher parallelism compared with the DLMS algorithm. Also utilized the inherent parallelism in DBLMS algorithm to derive a highly concurrent systolic-like architecture for high-speed implementation of adaptive FIR filter. The proposed structure can provide higher throughput compared with the existing pipelined structures [17].

Another important implementation by HesamAriyadoost, Yousef S. Kavian, Karim Ansari-As, performance evaluation of LMS and DLMS digital adaptive FIR filters by realization on FPGA. In this design realization of adaptive digital FIR filters on a single FPGA chip were presented and the performances of LMS and DLMS algorithms were compared in terms of chip area utilization and filter critical path time. Compared the number of utilized ALUTs for implementing 2-Tap, 4-Tap, 8-Tap, 16-Tap and 32- Tap LMS and DLMS adaptive FIR filters also the total number of utilized registers for implementing LMS and DLMS adaptive FIR filters. The DLMS adaptive FIR filters need more registers than LMS adaptive FIR filters for providing the delay lines. And finally compares the maximum frequency of LMS and DLMS adaptive FIR filters using the critical path time, the critical path of LMS FIR filters are longer than the DLMS FIR filters [18].

From review of various paper it is observed that most of the researchers have used systolic architecture for the multiplier design, matrix multiplication & many DSP application like RLS algorithm, LMS algorithm and FIR filter. Researchers compared the different architecture of LMS algorithm and obtained improved result in comparison with conventional method.

Therefore in order to perform multiplication more accurately and efficiently use of systolic architecture for design of adaptive FIR (finite impulse response) filter using DLMS algorithm, is a better solution.

III. APPLICATIONS

- As Adaptive equalization.
- Noise cancellation In Counters.
- System identification.

IV. CONCLUSION

This paper about systolic architecture can be used for the design of multiplier, matrix multiplication & many DSP applications like RLS algorithm, LMS algorithm and FIR filter. Low adaptation delay architecture for implementation of DLMS adaptive filter is achieved by using an efficient implementation of systolic architecture. By involving the concept of pipelining and parallel processing into systolic architecture the adaption delay, chip area and power consumption is reduce by a significant factor. Systolic architecture of DLMS algorithm designed using pipeline concept and implemented and achieved the improved result as compared with conventional method.

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