International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 3 Issue: 5 155 – 158

Review Paper on DDR3 SDRAM Controller for High Efficiency

Ms. Minal N. Kagdelwar
4th sem M. Tech Electronics Engg.
KITS, Ramtek
Maharashtra, India
E-mail: minu610kagdelwar@gmail.com

Mrs. Priti S. Lokhande
Dept. of EE,
KITS, Ramtek
Maharashtra, India
E-mail: pritimay06@yahoo.co.in

***Abstract*—** The demands and needs for faster and low cost memories are increasing per individual day. Therefore, a higher performance DRAM is required by the market due to increasing bandwidth of networks and the rise of high-capacity multimedia content. Synchronous Dynamic Random Access Memory (SDRAM) has continually evolved over the years to keep up with ever-increasing computing needs. The latest addition to SDRAM technology is DDR3 SDRAM. DDR3 SDRAM or Double Data Rate Three SDRAM is the 3rd generation of DDR memories that meets these demands in computing and server systems are used for high bandwidth storage of working data of a computer and other digital electronic devices. DDR3 Memory Controller is the interface between DDR3 memory and user. The memory controller manages the dataflow going to and from the main memory. It discusses the overall architecture of the DDR3 controller along with the detailed design and operation of individual sub blocks. To achieve high performance at low supply voltage and reduce power consumption, this work introduces new functions and describes their implementations. The focus of this paper is to minimize the delay and power and thus increasing the device throughput using pipelining in the design.

Keywords- *SDRAM (Synchronous Dynamic Random Access Memories), VHDL, XILINX.*

*****

I. INTRODUCTION

As a continuous increase in system bandwidths, memory technologies have been improved for higher speeds and performance. DDR SDRAM controllers generate very precise sequences of addresses, commands and data while observing a myriad of timing requirements. The next generation family of Double Data Rate (DDR) SDRAMs is the DDR3 SDRAM. DDR3 SDRAMs or Double Data Rate Three Synchronous Dynamic Random Access Memories offer plentiful advantages compared to DDR1 and DDR2. In general, double data rate memory provides source-synchronous data capture at a rate of twice the clock frequency. DDR3 devices provide a 30% reduction in power consumption compared to DDR2, principally due to smaller die sizes and the lower supply voltage. These DDR devices consumes lower power, operating at higher speeds, offer advanced performance (2x the bandwidth), and come in larger densities. DDR3 devices also offer other power conservation modes like partial and self-refresh. DDR3 delivers significant performance and capacity improvements over older DDR2 memory.

Technically, DDR3 SDRAM is a high speed synchronous dynamic random access memory with eight banks [1]. Access to different banks may be overlapped. The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation as compared to DDR2 SDRAM uses 4n architecture. Due to diverse signalling voltages, timings, and other factors, the accompanying interface techniques used by DDR3 SDRAM is not directly companionable with any earlier type of random access memory (RAM).

The ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth [2] or peak data rates [3] is the prime benefit of DDR3 SDRAM over its immediate ancestor DDR2 SDRAM. With two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed in megabytes per second (MB/s). As 64 bits data can be transferred at a time per memory module, DDR3 SDRAM gives transfer rate of (memory clock rate) * 4(for bus clock multiplier)*2(for data rate)*64(number of bits transferred) /8(number of bits/byte).

The structure of this paper is as follows: section II, describes the types of memory controllers, Section III discusses the overview of the memories, Section IV discuss about the proposed software design architecture. Finally, conclusion in section V.

II. TYPES OF MEMORY CONTROLLERS

A. DDR1 SDRAM Controller

A further advance in SDRAM memory technology is the Double Data Rate-SDRAM, or simply DDR SDRAM. After the DDR2 took its place, DDR became referred to as DDR1. The DDR memory works as same as its name point toward “double data rate.” This is achieved by transferring data twice per cycle, i.e., on both the rising and then the falling edge of the clock signal. SDRAM memory technologies were transferred data after one complete clock pulse as opposed to DDR1 [4]. Figure 1 shows the SDR and DDR data transfer with respect to the clock.

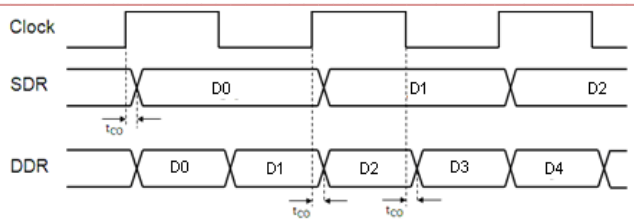

Figure 1: SDR and DDR timing diagram

B. *DDR2 SDRAM Controller*

DDR2 was introduced in the midst of 2003 as a successor to DDR1. DDR2 SDRAM offers greater bandwidth and density along with a reduction in power consumption. DDR2 allows higher bus speed and requires lower power by running the internal clock at half the speed of the data bus. Like all SDRAM implementations, DDR2 stores data in memory cells that are activated with the use of a clock signal to synchronize their operation with an external data bus. DDR2 runs with power line voltage of 1.8 volts against 2.5 volts for DDR1 SDRAM. Although this represents a drop in voltage of 72%, this would result the power consumed by approximately 50% for the same circuit. DDR2 has also been improved in the operating speed. Prior to working, DDR2 must be initialized first.

C. *DDR3 SDRAM Controller*

The third generation memory introduced in 2007 as the natural inheritor to DDR2 is DDR3. DDR3 core has an 8n-prefetch (where n refers to the number of banks per rank) as every read access to the memory requires a minimum of 64 bits (8 bytes) of data to be transferred. To stand the heating properties of the higher frequency, the voltage level was let down to 1.5 V. With earlier versions of RAM, DDR3 is both electrical and physically incompatible. Another interesting thing about DDR3 architecture is that it has a memory reset option and by using this reset option; DDR3 lets the memory to be cleared. Other memory types not having reset option will have indeterminate memory state after a system boot up. It is advantageous because this feature will outcome in a more stabilized memory system.

III. OVERVIEW

SDRAM was developed in the early 1990s to solve a problem that began picking up as computers and systems became more influential and complicated. Old DRAM used an asynchronous interface, which means it operated self-reliantly of the processor—which was not ideal if the memory couldn't keep up with all of the requests the processor made of it. SDRAM modernized this process by synchronizing the memory's responses to control inputs with the system bus, allowing it to line up one process while waiting for another. In such way, computers could execute tasks much more quickly than had previously been possible, and was the memory standard in computer systems by the end of the 1990s.

Around 2000, a new and fresh interface method was technologically advanced called double data rate (or DDR), letting the memory transfer data on both the rising and falling edges of the clock signal, giving it the capability to move information nearly twice as quickly as with regular SDR SDRAM. There was another side benefit to this change as well: It meant memory could run at a lower clock rate (100-200MHz), using less energy (2.5 volts- as DDR1 uses), and achieve faster speeds (transfer rates of up to 400 MTps).

Even though the concept of synchronous DRAM has been known since at least the 1970s and was used with early Intel processors, it was only in 1993 that SDRAM began its path to worldwide acceptance in the electronics industry. In 1993, Samsung introduced its KM48SL2000 synchronous DRAM, and by 2000, SDRAM had replaced fundamentally all other types of DRAM in modern computers, because of its superior performance. Parallel operations on different banks are allowed in the SDRAMs, due to the multi-bank architecture and burst read/write mode. By scheduling the memory access to each bank, high memory bandwidth can be attained.

In the applications of interactive programming systems, an address-conversion method which increases the memory bandwidth by 50% was presented by H. Kim [4]; Jaspers [5] suggested mapping of video data units into the memory in harmony with the information of actual data access consequences and he incorporated access to the memory banks; Memory management solutions for H.264 HDTV Decoder applications was provided by Zhang [6] and Zhu [7], which increases memory bus proficiency nearly by one third using techniques such as frame buffer arrangement and page break optimization.

These hard work stated above altogether are under the supposition that consecutive data access arrangements are predictable and thus data could be stored and regained at the formerly recognized address location of the memory. Nevertheless, this technique is not relevant to the arbitrary data access requisite in networking structures. T. Mladenov [8] was capable to evade unnecessary swapping between rows by reforming the addresses, thus increasing the memory proficiency for arbitrary access. Moreover, this technique is greatly reliant on the access pattern and the performance progress is uncertain.

The presented study aims the above deficiencies by discovering precise DDR3 SDRAM memory controller architecture that permit very accurate application of the DDR3 memory bandwidth and will be using pipeline processing to increase the speed measure.

IV. PROPOSED SOFTWARE DESIGN ARCHITECTURE

The DDR3 SDRAM uses double data rate architecture to achieve high-speed operation. The double data rate architecture is 8n-prefetch architecture with an interface intended to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM consists of a single 8*n*-bit-wide, one-clock-cycle data transfer

at the internal DRAM core and eight corresponding *n*-bit wide, one-half-clock cycle data transfers at the I/O pins.

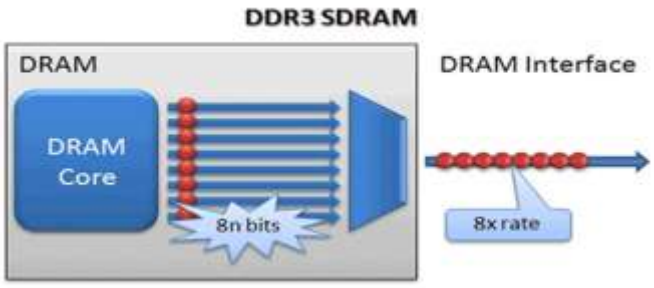

Figure 2: DDR3 SDRAM with 8-bit data rate

A. *Proposed architecure of DDR3 SDRAM*

The proposed architecture of DDR3 SDRAM controller is shown in figure 3.

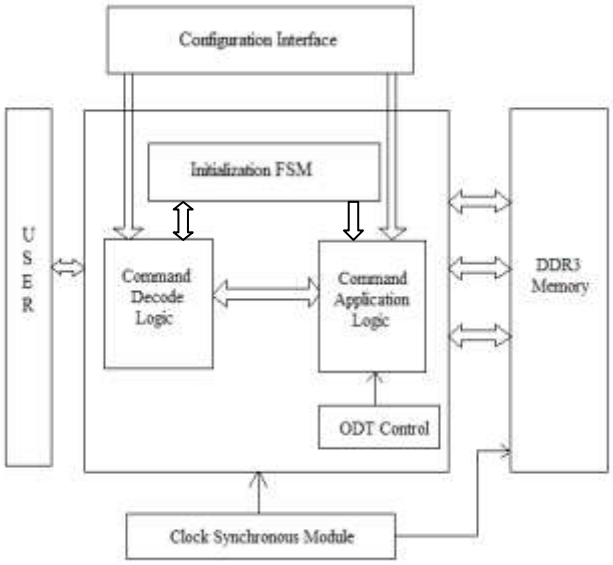

Figure 3: DDR3 SDRAM Controller Block Diagram

DDR3 SDRAM architecture is designed with three stage queue depth command Pipeline Module, Full functional State Machine, ODT (ON-Die Termination) control, clock module, configuration interface, and DDR3 memory.

SDRAM is high-speed Dynamic Random Access Memory (DRAM) with a synchronous interface. The proposed architecture is fully pipelined which allows fast data rates. Double Data Rate Three (DDR3) SDRAM Controller Core is designed for use in applications requiring high memory throughput, high clock rates and full programmability. The core accepts commands using a simple local interface and translates them to the command sequences required by DDR3 SDRAM devices. The controller core also performs all initialization, refresh and power-down functions. The core uses bank management modules to monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays. Up to 32 banks can be managed at one time. DDR3 SDRAM is formed with 8 banks and banks are addressed with rows and columns. The number of rows and columns depends on the configuration of the memory and size.

I. *Full Functional State Machine*

When system leaves the reset state, controller Core of DDR3 SDRAM handles the initialization of the SDRAM. The initialization state machine issues the appropriate sequence of command to initialize the memory devices. It also handles the periodic refresh operations to the SDRAM after initialization. SDRAM Controller provides an interface that allows an external process or logic to drive the SDRAM memory device initialization sequence.

II. *Address and Command Decode*

When the state machine wants to issue a command to the memory, it asserts a set of internal signals. The address and command decode logic turns these into the DDR specific RAS/CAS/WE commands.

Table 1: DDR3 SDRAM commands

Step	Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
1	Load Mode	L	L	L
2	Auto Refresh	L	L	H
3	Precharge [1]	L	H	L
4	Bank Activate	L	H	H
5	Write	H	L	L
6	Read	H	L	H
7	No Operation/IDLE	H	H	H

III. *Bank Management Logic*

The bank management logic keeps track the current state of each bank. It can keep a row open in every bank in your memory system. The state machine uses the information provided by this logic to decide whether it needs to issue bank management commands before it reads or writes to the bank. The controller always leaves the bank open unless the users requests an auto-precharge read or write. The periodic refresh process also causes all the banks to be closed.

IV. *Self-Refresh and Power-Down Commands*

This feature allows you to direct the controller to put the external memory device into a low-power state. There are two possible low-power states: self-refresh and power down. The controller supports both and manages the necessary memory timings to ensure that the data in the memory is maintained at all times.

V. *Auto-Precharge Commands*

The auto-precharge read and auto-precharge write commands allow you to indicate to the memory device that

this read or write command is the last access to the currently open row. The memory device automatically closes (auto-precharges) the page it is currently accessing so that the next access to the same bank is quicker. This command is particularly useful for applications that require fast random accesses.

VI. DDR3 Dynamic On-Die Termination

To ensure high signal quality required in a high-speed data transfer system, a processing technology is needed to control signal reflection with greater precision. For optimum signalling, a typical dual-slot system will have a module terminate to a LOW impedance value (30Ω or 40Ω) when in an idle condition. When the module is being accessed during a WRITE operation, greater termination impedance is desired, for example, 60Ω or 120Ω. Dynamic ODT enables the DRAM to switch between HIGH or LOW termination impedance without issuing a mode register set (MRS) command. This is beneficial because it improves bus scheduling and decreases bus idle time.

V. CONCLUSION

By using the new features of DDR3 SDRAM and using software XILINX 8.1i, the goal is to simplify the proposed design process for DDR3 SDRAM which synchronizes the transfer of data between DDR RAM and external peripheral devices like host computer, laptops and so on. As the data rate is being doubled than DDR1 and DDR2, faster data transmission with less delay is expected and thus enabling higher bandwidth. The main objective of the paper will be fulfilled by replacing parallel processing by pipelined stages architecture of DDR2 SDRAM Controller to reduce delay.

REFERENCES

[1] DDR3 SDRAM Specification (JESD79-3A), *JEDEC Standard*, *JEDEC Solid State Technology Association*, Sept. 2007.
[2] Xin Yang, Sakir Sezer, John McCanny, Dwanyne Burns, "DDR3 Based Look-up circuit for High Performance network Processing", IEEE 2009, pp 351-354.
[3] www.altera.com/literature/ug/ug_altmemphy.pdf, External DDR Memory PHY Interface Megafunction User Guide (ALTMEMPHY), accessed on 23 Feb. 2009.
[4] H. Kim, et al, "High-Performance and Low-Power Memory-Interface Architecture for Video Processing Application", *IEEE Transactions on Circuit and Systems for Video Technology*, Vol. 11, Nov. 2001, pp. 1160-1170.
[5] E. G. T. Jaspers, et al, "Bandwidth Reduction for Video Processing in Consumer Systems", IEEE Transactions on Consumer Electronics, Vol. 47, No. 4, Nov. 2001, pp. 885- 894.
[6] N. Zhang, et al, "High Performance and High Efficiency Memory Management System for H.264/AVC Application in the Dual-Core Platform", *ICASE*, Oct. 2006, pp. 5719-5722.
[7] J. Zhu, et al, "High Performance Synchronous DRAMs Controller in H. 264 HDTV Decoder", Proceedings of International Conference on Solid-State and Integrated Circuits Technology, Vol. 3, Oct. 2004, pp. 1621-1624.
[8] T. Mladenov, "Bandwidth, Area Efficient and Target Device Independent DDR SDRAM Controller", Proceedings of World Academy of Science, Engineering and Technology, Vol. 18, De. 2006, pp. 102-106.
[9] J. Bhaskar "A VHDL Primer", *3rd Edition ,Pearson Education.*
[10] Micron 1GB DDR3 SDRAM, *Micron Technology Inc.*, 2006**.**
[11] Micron Technical Note TN41-04: DDR3 Dynamic On-Die Termination Introduction.
[12] Design of Low Power Double Data Rate 3 Memory Controller with AXI compliant' International journal of engineering and advanced technology (IJEAT) Vol.1, Issue 5, June 2012.