

All-Optical Packet Processing in Optical Network

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Abstract— Next Generation Networks demand quick access of data from all around the globe, thus populating backbone network with heavy data traffic. All-optical network is capable to handle such ever increasing load with reduced complexity. In this scheme the processing is done completely in optical domain employing pure optical devices. The optical packet includes the control information (header) and data bits (payload). Semiconductor Optical Amplifier and optical couplers are employed for header extraction. Header and routing table information is converted in pulse Position format for ease of processing. This provides high speed processing of optical packet with less optical complexity and reduced routing table. Then it concentrate on the packet forwarding technique, which includes the optical pulse matching logic, and then followed by the simulation part, which shows the implementation in MATLAB Simulink. Finally, concludes the topic with future scope for optical processing in high speed world.

Keywords - All-optical processing, header extraction, optical routing table, packet forwarding technique.

I. INTRODUCTION

With the upcoming era of technology, there is a great demand of high speed transmission of data. In this millennium, we are viewing tremendous rise in the telecommunication industries that have far-reaching effect on day-to-day data transmission requirements. The data transport is not only because of the voice traffic but is primarily fueled by now-a-days data centric technologies. This increase in data should be instantly available across the globe and must be reliable. To cope with ever increasing data traffic the under laid network must be able to handle few Tera bits of data per second. During transmission user data is encapsulated with destination address (Header) into a packet, which follows the shortest path determined by the router. Therefore core interest of this work is to deal with working of optical routers.

Ascending engineering boosts the internet traffic, doubling it every four to six months thus we can say that Moore's law is also applicable for data traffic. To meet the requirements we adopted broadband access technologies such as Digital Subscriber Link (DSL), cable modem, but the links may merely aid the load. Also, the silicon technology is approaching its physical limits. Use of VLSI technology for packet forwarding may support the growth not more than 10-15%. At this juncture, there is need of high data rate transmission; this provides great scope for all-optical packet processing in information networking.

This work proposes a framework which establishes high data rate transmission with least latency and data routing from source to destination. The technique used in designing all-optical router is discussed in the following sections along with the simulation and result discussion.

II. ALL-OPTICAL PACKET PROCESSING

Rapidly growing internet traffic is one of the major driving forces for deploying all-optical-based communication systems that offer a much greater transmission bandwidth, higher end-to-end reliability and cheaper installation cost when compared with the copper-wire, optoelectronic-based and satellite communication systems in long-haul transmissions.

A. Current Issues and Techniques in Optical Networking

In optical fiber based systems, high transmission capacity is achieved by employing wavelength division multiplexing (WDM) and optical time division multiplexed (OTDM) techniques [1]. In the ultrafast dense-WDM (DWDM) and OTDM networks [2,3], where the aggregate bit rate exceeds 100 Gbit/s, Optical-Electrical-Optical modules are not only costly but also impose the speed bottleneck beyond 40 Gbit/s owing to the limitations of processing speed of the electronic devices. In recent years, comprehensive research activities in the development of packet switching routers in the optical domain for ultrahigh-capacity photonic DWDM and OTDM networks are seen. The simplest is based on all-optical self-driven packet switching scheme with a predefined look-up routing table at the source router [4], where the header address is used to set the optical switches in the core router to the on/off states to ensure packet forwarding. Positioning of signal on time axis for header recognition [5] provides optical header recognition which uses a bank of all-optical mirror based correlators and a threshold detector for optical correlations.

B. Optical Core Network

With all-optical core network with N nodes, each node is identified by a unique decimal address which corresponds to $\{0,1,2,\dots,N-1\}$. In the core network, packets are routed from a source node to a target node via a defined shortest path following multihop. The incoming data packet, at the edge of the core network, is encapsulated with target node address to it for its designated node. The edge router converts the electrical packet into high speed optical packet at the bit rate of $1/T$, where T is duration of the bit. Binary address bits and clock pulse are placed as header which corresponds to the decimal address of the router.

Packet is determined by its header bits, therefore in packet processing, header processing plays a core role. As all-optical header processing is imperative to achieve a truly all-optical packet-switched network, different approaches have been demonstrated in [6-8]. In this work, a header processing scheme based on the Pulse Position (PP) has been employed, where the incoming packet header address

and the routing table entries are both converted into the PP format. This scheme provides reduced Routing Table size, and thus reduced header processing time. The latter is achieved by employing only a AND gate for pulse matching operation. In addition, the Pulse Position router offers multiple transmission modes.

C. Principle of All-Optical PP

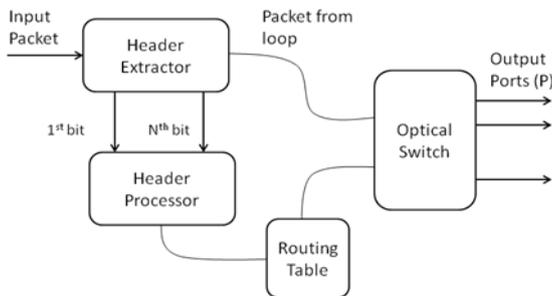


Figure 1. All-Optical Router Model

A 1×P PP based router block diagram is illustrated in Figure1. It comprises of header extractor module in combination with a serial to parallel converter and a common pulse-position routing table (PPRT). Logic unit and all-optical switches forwards the packet stored in the loop.

In Figure1; assume that a packet arrives at the input port of the node N. The input packet is cloned into two; one given for header extraction and another is kept in optical loop. The header bits include the port address and a clock pulse, address bit is fed to serial-to-parallel converter (SPC), and the latter is given for clock regeneration. A lens and mirror are used with a guided slow detector pulse, converts the serial pulses into parallel bits. Parallel output of SPC is then fed parallel to the input of Pulse Position-Address Conversion Module (PP-ACM) block. Switches and predetermined delay in PP-ACM converts the parallel signal into PP format. Pulse Position Routing Table (PPRT), is a PP converted routing table arranged in such a way that the output of PP-ACM pulse is used with optical AND gate drives the packet in loop to the respective port. The correlated output of AND gate determines whether the address is unicast, multicast or broadcast.

D. All-Optical packet Header Extraction

In order to transmit the packet from source to destination via all-optical routers, it is necessary to define the header. The header guides the payload for its further path to destination. In this scheme, the header of the packet is kept constant till the target edge node; therefore at the intermediate node only header bits are extracted from the packet for processing. Optical coupler is used to pullout part of power from the packet for header extraction.

All-Optical Header Extraction [9], includes modified semiconductor optical amplifier (SOA) and tunable delay tuned to provide a phase difference at the output of SOA. It should be kept in mind that, before the packet enters the header extraction module, a duplicate packet is held back in the optical loop, so that the same is transmitted to its respective ports.

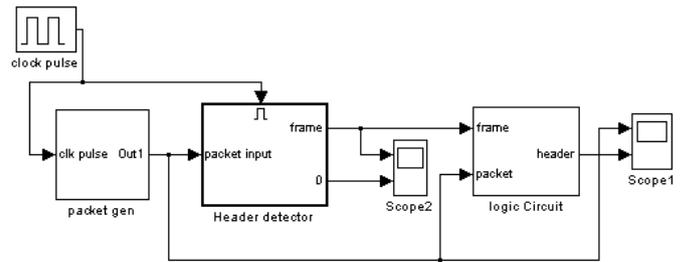


Figure 2. Simulation of header extractor in Simulink

The simulation model of header extraction is as shown in Figure 2. When the optical packet arrives at the node, it is then fed to optical coupler (C) to produce a duplicate packet at the other end. The optical coupler has power splitting ratio of 50:50; that is, it duplicates the signal with equal power factor. Now, one of the two output produced form C is given to semiconductor optical amplifier and another input is provided with a delay at other end of SOA. Thus one of the signals propagates in clockwise (CW) and another in counterclockwise (CCW) direction. Tunable fiber delay lines (FDLs) are used to introduce a delay between two pulses coming in opposite direction. Hence, the two counter propagating pulses arrive asynchronously at the SOA with time interval of Δt . For the header extraction part the following time relation is assumed, $\Delta t < \tau < \tau_s < \tau_h$, where τ_s is the carrier lifetime of the SOA, τ is the time spacing between the two pulses in payload and τ_h is time interval of pulses in header.

E. Serial to parallel converter

The output of header extractor is fed to Serial to Parallel Converter (SPC). The fundamental concept is to convert the series of bits into independent parallel signal using logical devices. There are several schemes proposed which uses SOA-MZI which increases the complexity. Ultrafast all-optical SPC [10] is used; which includes lenses and reflectors, reducing complexity. Layout of SPC is as shown in Figure3; this scheme exercises the conversion with the use of single optical clock. In this scheme, the incoming serial bits are simultaneously converted in parallel with periodically timed single bit pulse. This pulse can be derived from an optical clock pulse. The mirror used in the scheme is a low-temperature grown surface-reflection all-optical switches (LOTOSs).

A slow detector is basically a pulse generator which generates the pulse at an instance where all the bits are in single pulse window, and thus results in the reflection of parallel bits. Consider an incoming optical packet with an N bit (5 bits) header which is to be split into N parallel bits, then each bit is coupled with N different delay lines, where each line has a different amount of delay with bit separation t_h .

So, if we view all the lines then at the particular time instance say t_2 , we can extract all the bits from the delayed link.

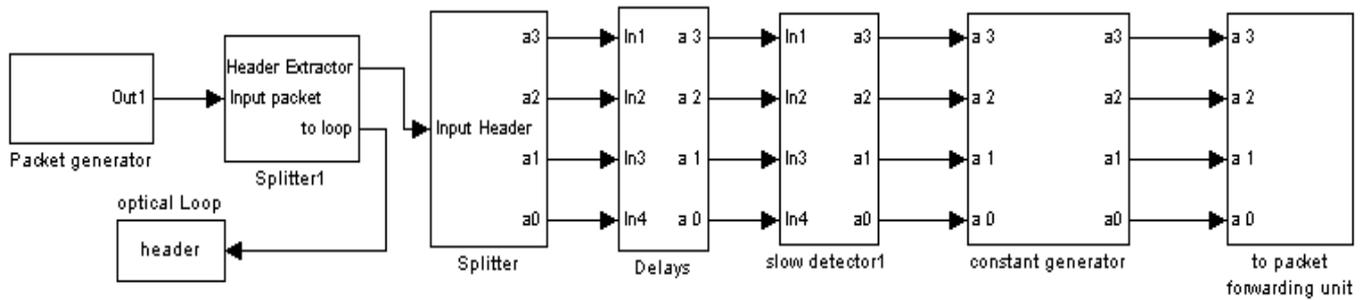


Figure 3. Packet detector and Serial-to-parallel converter

Therefore, there exists a time window that encloses all the header bits from 1 to N.

F. Packet Forwarding

The pulses produced at the output of serial-to-parallel converter is fed to PP-ACM [11], which in turn produces a pulse in address index, used for matching the port address in optical routing table. Pulse Position Routing Table is in predefined tabular format defined in three addressing index, as shown in table 1.

TABLE I. PULSE POSITION ROUTING TABLE

Address Pattern	Decimal value	Output Ports
0000	0	Port 1
0001	1	Port 2,3
0010	2	Port 1
0011	3	Packet dropped
0100	4	Port 2
0101	5	Port 3
0110	6	Port 1
0111	7	Port 3
1000	8	Port 2
1001	9	Port 1
1010	10	Port 1,3
1011	11	Port 3
1100	12	Port 1
1101	13	Port 2
1110	14	Port 1,2,3
1111	15	Port 3

Pulse matching block contains three AND gates and switches which delivers the packet at the output port. PP-ACM pulse is matched with the address index in PPRT, which drives the switches. The switch block comprises of simple 2D MEMS switches driven by the controlled output from AND gate. Optical switch directs the packet from the loop to the appropriate ports. The matching pulse in PPRT signal for different address index- E1, E2 and E3- determines connection type (unicast, multicast and multicast).

1) *Pulse Position Address Conversion Module*: Pulse Position Address Conversion Module is the assembly of blocks producing a result of single pulse representing the decimal value, which is an imitation of input header address. Input to this block is the signal from the serial to parallel converter, thus at each of the independent input interface we have header pulses defined as a_3, a_2, a_1 and a_0 as shown in figure 4.

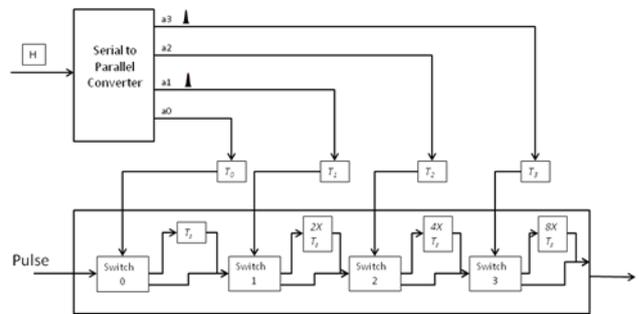


Figure 4. Pulse Position Modulation Address Conversion Module

SPC converts the sequence of header into parallel signals designated as a_3, a_2, a_1 and a_0 . Each converted signal is fed to the respective switches via delay unit. The delay is proportional to the processing time for switches. Switches used can be simple MEMS 2D switches. Each switch is connected with the delay unit of $2i \times \tau_s$, where $i=0,1,2,3$ and τ_s is the pulse duration in the routing table. Thus, switch determines the selection of delay unit and in turn depends upon the header bit position. Hence, if arrived pulse is high i.e. 1, then delay unit is selected based on the pulse position; and, if arrived pulse low i.e. 0, then the output omits the delay and goes directly to the next preceding switch. For example, if input parallel pulse is “1010”, this is denoted as a_3, a_2, a_1 and a_0 . Due to the arrangement of blocks, the end total is the pulse delayed by $10\tau_s$. Thus the scheme imitates the sequence at input with a pulse at address index as shown in figure 5.



Figure 5. PP-ACM output, position #10 for input “1010”.

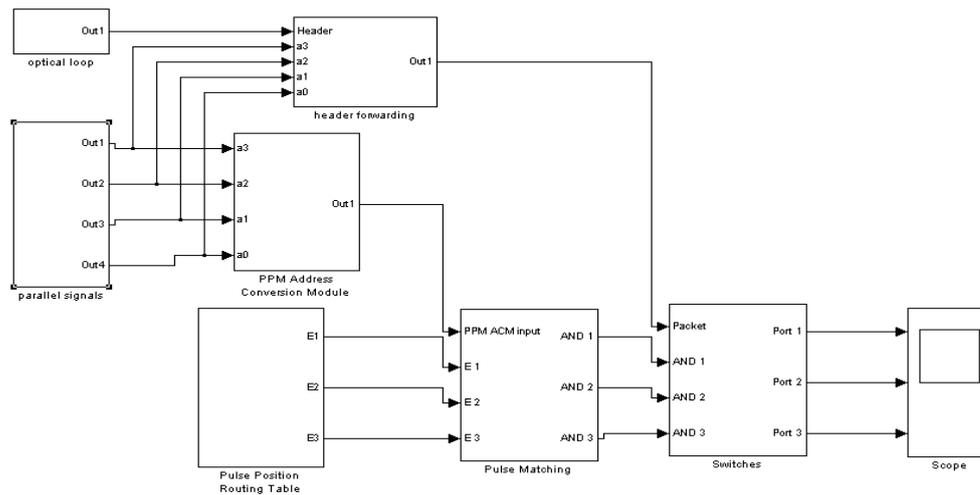


Figure 6. PP-ACM and Switching Logic.

PP-ACM produces the control signal, which is then fed to AND gates for correlation of pulses in routing table. The above scheme (figure 6) is simple and fast, but we have to maintain the signal pace.

III. SIMULATED OUTCOME

Each optical packet is encapsulated with header of 5 pulses; one is used as clock and rest four bits are used as address which is fully encoded to define the nodes/routers, whereas payload is considered as high data rate arbitrary pulses. The simulation is carried out in MATLAB Simulator. Figure 7 shows the packet format and the extracted header for processing. For ease payload is taken as any high bit rate arbitrary binary sequence.

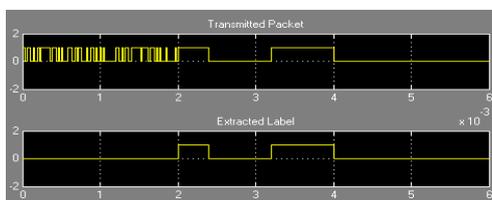


Figure 7. Optical Packet and separated Header

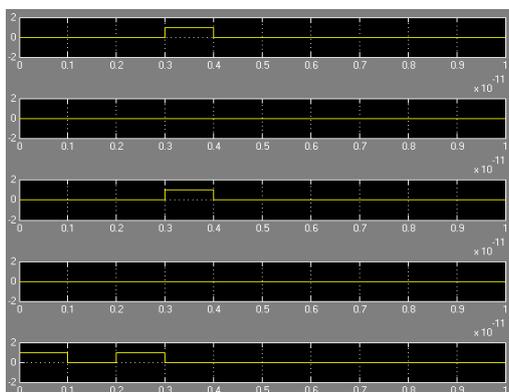


Figure 8. Output of SPC showing a₃, a₂, a₁ and a₀ pulses "1010"

SPC converts the incoming sequence into parallel pulses as shown in Figure8. Slow detector pulse determines the output of Serial-to-parallel converter. The routing table bit is predefined and decides the output port. The PP-ACM

pulse is then used as matching index in the routing table. Pulse matching is performed by exercising optical AND gate [1]. When the pulse is matched in the any of the AND gate, it drives the packet stored in the optical loop to the respective port via optical switches.

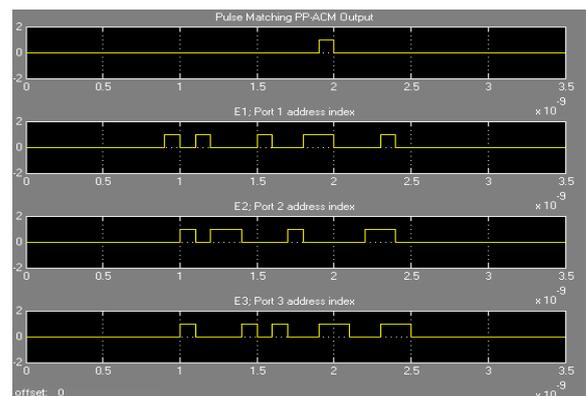


Figure 9. Output pulse of PP-ACM for matching with PPRT

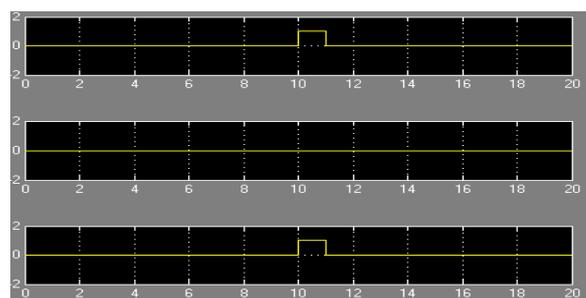


Figure 10. Two pulses generated after the match, used to drive the switch for packet forwarding

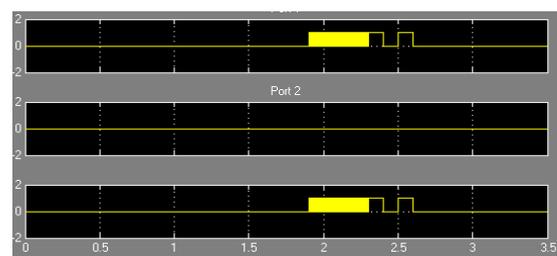


Figure 11. Multicast output of the All-optical Router.

Optical AND gate produces the signal which drives the switches, this signal can drive the output switch to any transmission mode. The switches then produce the output to respective port, and if there is no pulse matching then the packet is dropped.

IV. CONCLUSION

In this work, operation of PP node has presented, using a single bitwise header address correlation; the operation and result is performed in MATLAB Simulink simulator. This technique offers faster correlation time and overcomes the speed limitation imposed by non-linear elements. The payload is kept independent of processing, thus further increasing the flexibility.

In this proposed router, header processing has offered the advantages compared to existing logic-based processing such as, (i) it significantly reduces routing table size, thus improving the processing time (ii) Overcoming the slow response-time and recovery-time of the existing all-optical AND gates based on the SOA during header recognition. (iii) Offers enhanced scalability. (iv) Offers unicast, multicast and broadcast transmitting modes capabilities.

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