Improve Performance of Adaptive Multi-Modulus Frequency Divider by Pulse Triggered Flip Flop

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Abstarct :- A divider of frequency with minimal power & greater speed with multi modulus is elaborated along design of a PLL. In this document by making use of a ff initiated by a pulse is plowed by which a definite divider with 2 levels can improvise the frequency of function & deduce decadence of power. A constituent which is adaptive s formulated to be retained in a divider with great mode of saving in power. The frequency of a defined divider with 2 levels in accordance to CMOS of 130 nm process may attain 4 GHz. The basic decadence f power is division by 49 mode at 63 uW with frequency of 1 GHz or 156uW at 4 GHz. In a contrast of the counter of Johnson FD, frequency of a divider with 2 levels is improvised & so the proportion of optimization of power.

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I. INTRODUCTION

The divider of frequency often termed as divider of clock which can be pre scaler or scaler is a circuitry in which a frequency f_{in} is furnished as input & gives out the signal as outcome as:

$$f_{out} = \frac{f_{in}}{n}$$

Here n is taken as an integer. The exploitation of dividers of frequency is done by PLL for formulation of frequency which is in multiple count of frequency of reference. The implementation of FDs can be made for digital as well analog applications.

II. SINPLER ANAGLOG DIVIDER/AD

An elementary AFD is not much basic & is implemented for applications with high frequencies. The modern dividers which are digital are implemented in the IC technology & can function in the range of tens of GHz.

III. REGENERATION FREUENCY DIVIDER/RFD

A RFD often termed as miller divider of frequency & amalgamate the input of signal with thr signal of feedback from a mixer.
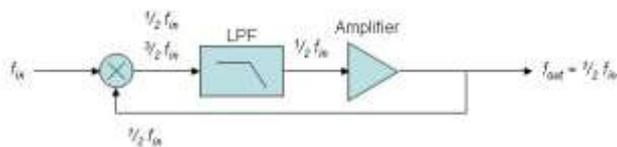

Figure 1 :- Diagram of RFD

A feedback signal is $f_{in}/2$. It is a defined type which furnish freuency of a type of contrast which is $f_{in}/2$ & entirety, $3f_{in}/2$ which is theh outcome produced by mixer. The filters at a minimal pass shifts the freuency of high range & frequency of $f_{in}/2$ which is intensified after invading a feedback to mixer.

IV. FREQUENCY DIVIDER OF LOCKED INJECTION

The oscillator which runs in a free state can compute the signals with frequencies to a bit greater value in accordance to it that is having a propensity of oscillation with progression in the signal that is provided as input. So the dividers of a particular frequency were found sensitive in improvisation of tv.

It also functions in accordance to the oscillators that are locked by injection in the dividers of frequency. Also the frequency of signal of input is in terms of oscillators that are running freely in frequency.

The dividers of frequency possess capability to attain a level of power at the same instance which is minimal than that of dividers of frequency which are broadband, below which the least lock domain is present of tank of oscillator. The range of locking of ILFD is in accordance to the Q which is factor of quality of the tank. In the structure of IC, the process of touch in ILFD is to the diversities. Some attention is requires to assure the scope of tuning of the driven circuitry which should lie in domain of range of locking of input of ILFD.

V. PROBLEM STATEMNT

The FD (Frequency Divider) is a standout amongst the most discriminating blocks in phase locked loops[1,2] (PLLs, figure 1). With the advancement of devices and the scaling of CMOS process technology, low power utilization and high working frequency are key designing characteristics of frequency divider. The progressing PLL in system on chip (SOC) scatter under 7mW[3], while a solitary frequency divider would cost more than 1.0mw[4]. For the most part, it is regular for PLLs to contain a few of these dividers, which implies that more than 30% power consumption is involved by the divider.
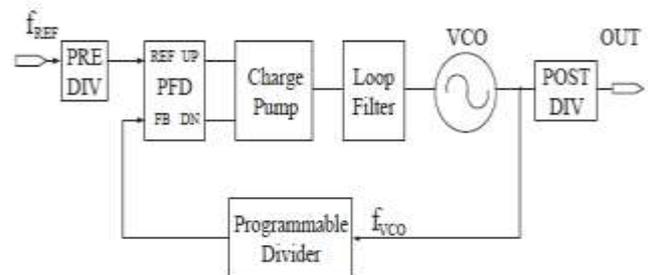

Figure 2: PLL- Block Diagram

The simplest divider of frequency is the counter that is programmable & attains minimal decadence of power & a range of modulus. Also it has a minimal frequency of operation. It is kept in notice that end goal to further enhance operating frequency while as yet keeping up the power efficiency, we adjust the design principle of programmable pulse swallow frequency divider, cut traditional architecture of Johnson counter into two stage divider which will both accomplish high operating frequency and low power dissipation. A component has been proposed to set the frequency divider in the best power saving mode.

VI. BUILDING DESIGN OF MULTI MODULUS FREQUENCY DIVIDER

The design of a modulus that can be multi & programmed is suggested in 4&5, utilizing cascaded static DFF based 2/1 divider cells or is divided by 2/3, is a structure of multi modes which is of

type generic. Then again, they may not accomplish great power efficiencies.
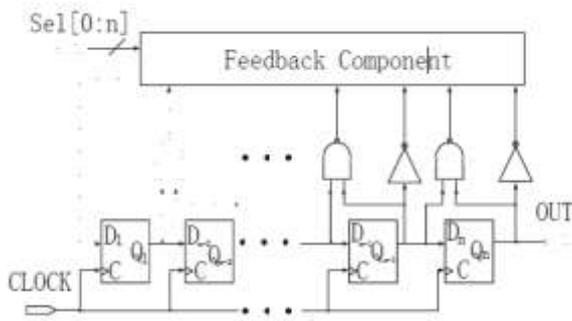

Figure 3:- The Johnson Programmable Structure

Changing the binary programming values of the feedback component, the division ratio might extend from 1 to 2n. In any case, with the increase of division ratio n, more DFF are necessary and the logic of feedback component would significantly increase. For this situation, the delay of feedback chain will expand and operating frequency will be compelled. The drawbacks that we specified above have confined the application of Johnson counter.
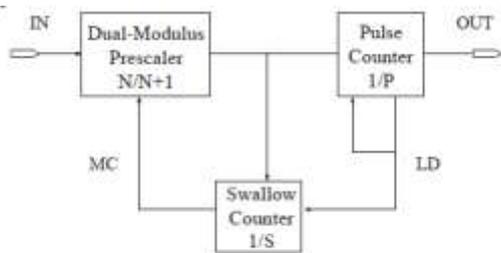

Figure 4:- Programmable Type Pulse Swallow Frequency

It comprises of a scalar which is on pre time & dual modulus along 2 counters that are programmed, presented as counter of pulse & swallow. The proportion of division D of the divider that is programmed is calculated as,

$$D = (N+1)S + (P-S)N$$
$$= NP + S$$

Double modulus presale works at high frequency, so that the operating frequency of pulse counter and swallow counter is relatively low, which make the overall divider dissipate less power and operate at high frequency. In any case, there is an extraordinary imperfection that the division ratio won't begin from 1, which additionally constrains the application of pulse swallow frequency divider. A digitally controlled injection locked multiple modulus frequency divider is displayed in [7], which is fit for high operating frequency. In any case, it is difficult to work over a modulus range. In this paper, consolidating the benefits of these structures above, we plan a novel two stage frequency divider that cannot just accomplish high operating frequency and low power dissipation, additionally perform wide modulus go that begins from 1 to 2n two stage divider. The Johnson counter is separated by two parts, the dynamic power utilization of a DFF is composed as takes after,

$$P_d = C \cdot V^2 \cdot f$$

Where f is the clock of DFF, C is the whole of capacitor. Under the particular process, the V and C are altered. Ignoring the temperature effect, the power is proportional to the f. The second divider works at lower frequency. For this situation, the total dynamic power utilization of two stage dividers will drop down. Since the long

feedback chain is part into two short chains, the delay of the first divider will decrease, which enhances the operating frequency.
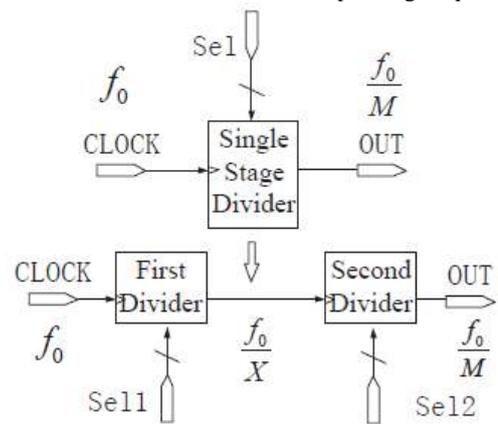

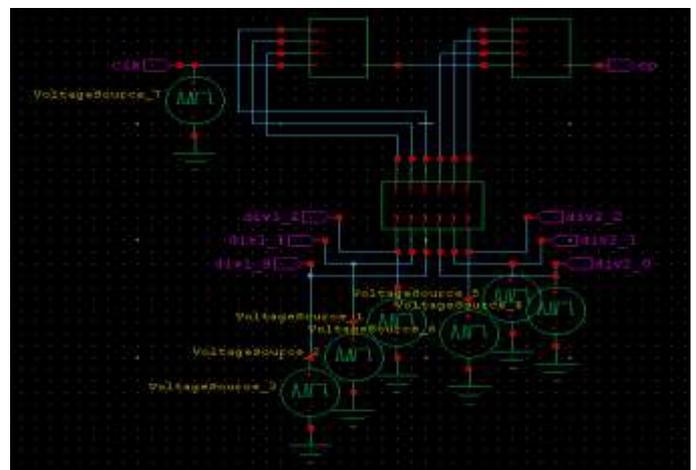Figure 5:- Frequency Divider (Two Stages)

Fig 6:- Frequency divider tanner design

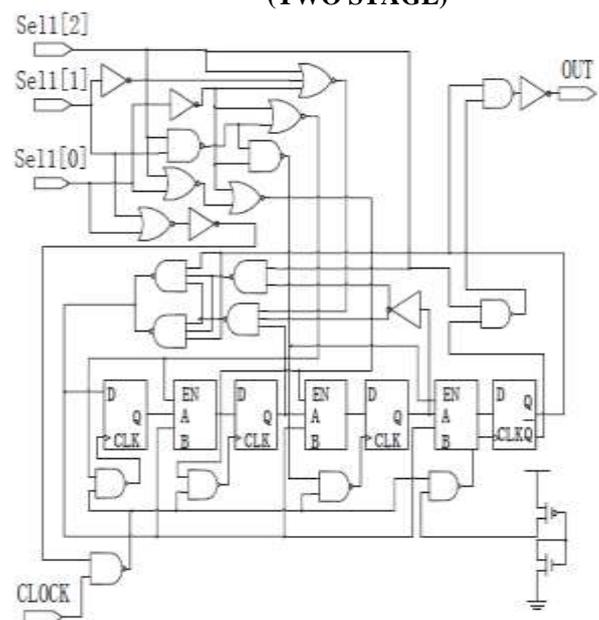## VII. INSTANTIATION OF FREQUENCY DIVIDER (TWO STAGE)

Figure 7: Programmable FD (Frequency Divider) Divide By 7

Utilizing the design principle of segment 3.1, we display a two stage structure that the maximum division ratio is 49. As figure first and second division ratios can range from 1 to 7. Clock is the input signal, sel1[0:2] are binary control values, each DFF is trailed selector. By setting the EN to 1 or 0, the selector chooses distinctive data.
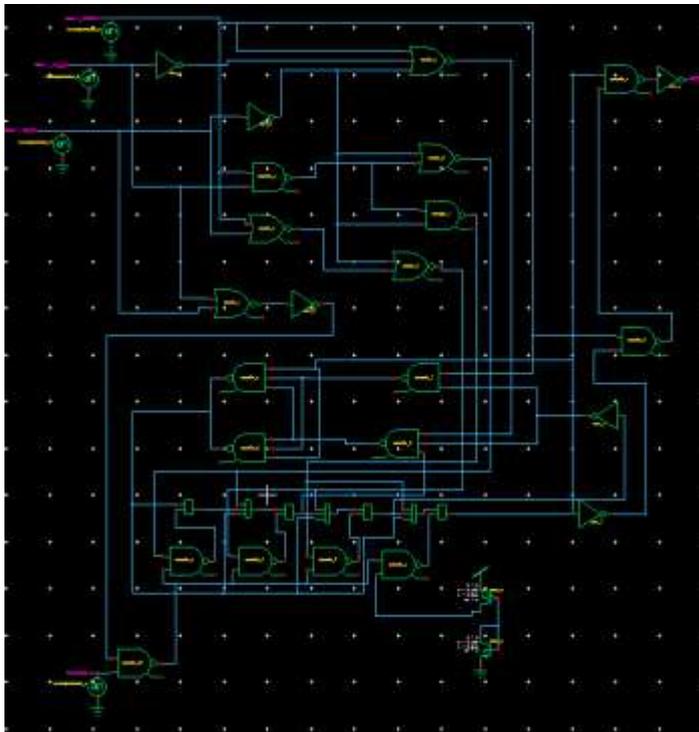

Figure 8:- FD (Frequency Divider) Divide By 7 Tanner design

3.4 ADAPTIVE COMPONENT

Accepting the first divider is situated to divide by x mode, and the second divider is situated to divide by M/X mode. An upgraded arrangement is let X>M/X dependably, which diminish the power consumption to lowest. For the most part, to maintain the relationship in the middle of X and X>M/X, with respect to the change of X, we proposed an adaptive block to accomplish this capacity.
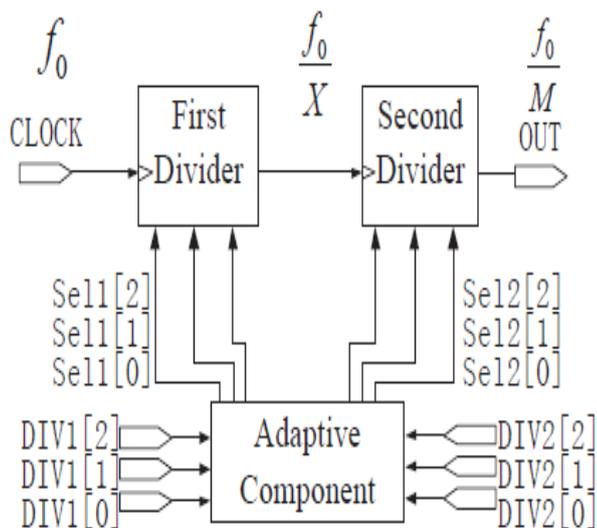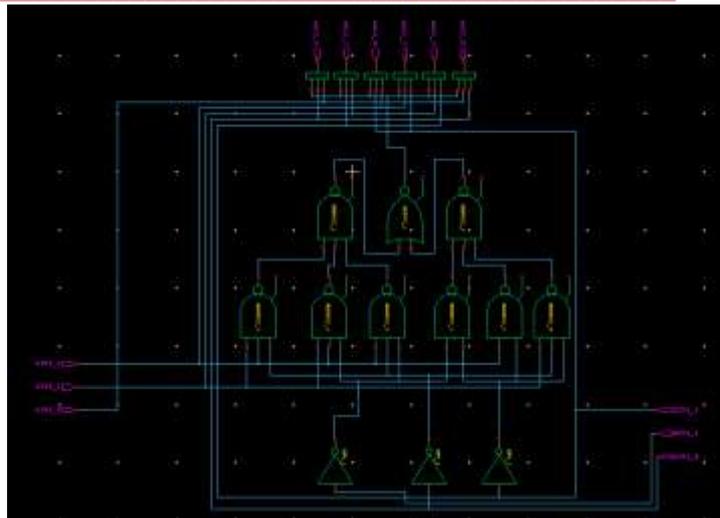

Figure 9:- Programmable FD (Divide By 49)

Figure 10:- Adaptive component design by tanner tool

VIII. INSTANTIATION OF ADJUSTABLE COMPONENT

The adjustable component is really a selector. It constrains the division ratio of the first divider larger than proportion of division of proceeding divider. The frequency of input of the second divider would be the relatively lowest, so the aggregate absorption of power will be minimal.
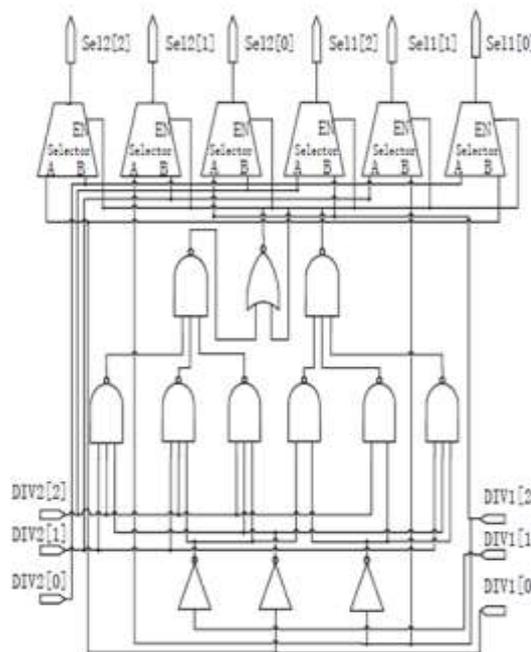

Figure 11:- Adaptive component

Every divider contains three selecting signals, DIV1[2], DIV1[1], DIV1[0] relating to the first divider, DIV2[2], DIV2[1], DIV2[0] comparing to the second divider. By encoding the six signals together, we can accomplish the capacity that when the EN is situated to be 1, the six signals will to the corresponding divider, when the EN is set to 0, the six signs will be reversed to input to another divider.

IX. PROPOSED METHODLOGY
PULSE TRIGGERED (MASTER-SLAVE) FLIP FLOPS (F/F)

This terminology of triggered pulse indicates that data is invaded into raised side of pulse of clock though the outcome doesn't shadow state of input till the failing side of pulse of clock. The ffs of this type are crucial to any variation at stage of input when amid pulse of clock is kept high & input is also proceeding. The ffs which are triggered by pulse are of 3 types which are J-K, S-R & D. below are their symbols of logics. They don't possess any input reflector which his dynamic at clock of input though the images of outcome on that side is delayed.
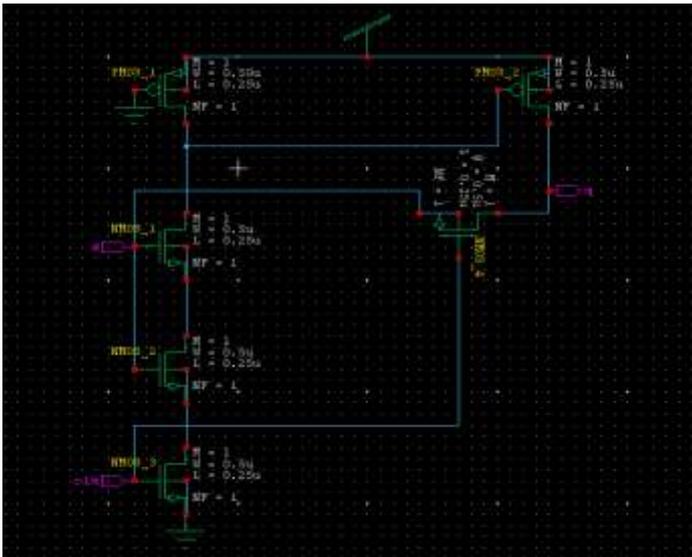

Figure 12:- Design ff triggered by pulse

We replace ff D by the one triggered by pulse . This change make the delay and power reduction .

X. RESULTS
EXIXTING DESIGN
Design waveform are for frequency divider by use D flip flop . D flip flop is using in frequency divider of first and second both.
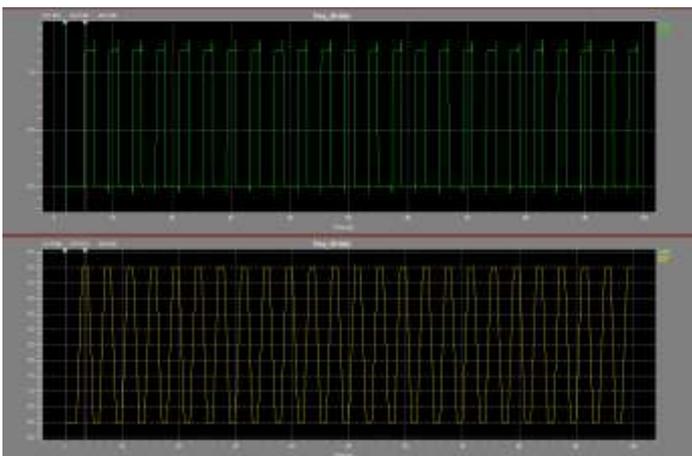

Figure 13:- Existing design waveform for DFF

Average power consumed -> 1.569759e-003 watts
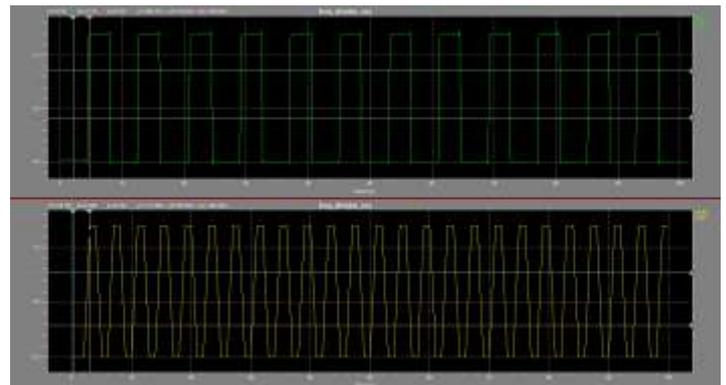Delay :- 3.38 ns

PROPOSED DESIGN

Figure 14:- Proposed Design for PFF

Average power consumed -> 1.405284e-003 watts.
Delay :- 2.85ns

5.3 COMPARISON TABLE

	Power (Watts)	Delay (ns)
EXISTING DESIGN	1.569759 e-003	3.38 ns
PROPOSED DESIGN	1.405284 e-003	2.85ns

Table 1:- Comparison Table

XI. CONCLUSION & FUTURE SCOPE

In this Thesis, we suggested novel pulse triggered Flip Flop (F/F) by utilizing structure of two stages. The suggested divider is made optimal for greater frequency & minimal power operation in the architecture level to build operation frequency and also to minimize delay. By diminishing input frequency of second divider, aggregate power consumption of two stage divider would be adequately decreased. Operating frequency is enhanced in view of lessening of logical chain. The trial experiments demonstrate that two stage frequency divider (FD) will accomplish great execution in both sides of low power consumption and high operating frequency, while it performs wide modulus range also. Moreover, clock gating technology can be decision for to reduce in operating frequency in sections of logic, as we known, the execution of clock gating shifts from EDA TOOLS, which drives particular method unacceptable in designing of PLL.

In the future we can improve the results by apply GDI technique for power quality improvement. For reduce the delay and area we can reduce number of transistors . After reduce the number of transistor the area will also reduce .

REFERENCES

[1] Ma Zhuo, ZHAO Zhenyu, GUO Yang, et al, A Method of Balancing the Global Multi-Mode Clock Network in Ultra-large CPU, Springer Publishing, p.1-7, (2013).

[2] Ma Zhuo, Guo Yang, Xie Lunguo, et al, A noise rejective VCO with build-in active LC filter, Proceeding of the 9th IEEE International Conference on ASIC, p.598-601, (2011)

[3] Shih-An, Yu, Peter Kinget, A 0.65V 2.5GHz Fractional-N Frequency Synthesizer in 90nm CMOS, IEEE International Solid-State Circuits Conference on Digest of Technical Papers, p.304-604, (2007).

[4] Chi-Sheng Lin, Ting-Hsu Chien, Chin-Long Wey. A 5.5-GHz 1-mW Full-Modulus-Range Programmable

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Frequency Divider in 90-nm CMOS Process, IEEE Transactions on Circuits and Systems II, 58(9), p.550-554, (2011).

[5] Wenguan Li, Honglin, ChenLei Shi, A 4.5-GHz 256□511 multi-modulus frequency divider based on phase switching technique for frequency synthesizers, IEEE International Conference of Electron Devices and Solid-State Circuits, p.1-4, (2010).

[6] Wenguan Li, Honglin Chen, Ruohe Yao, A 5.5-GHz multi-modulus frequency divider in 0.35□m SiGe BiCMOS technology for delta-sigma fractional-N frequency synthesizers, International Conference on Microwave and Millimeter Wave Technology, p.1937-1940, (2010).

[7] Joonhee Lee, Sunghyun Park, SeongHwan Cho, A 470□W 5-GHz Digitally Controlled Injection-Locked Multi-Modulus Frequency Divider With an In-Phase Dual-Input Injection Scheme, IEEE Transactions on Very Large Scale Integration Systems, 19(1), p. 61-70, (2011).