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Implementation of Low Power and Area Efficient 2-Bit/Step Asynchronous SAR ADC using Successively Activated Comparators

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***Abstract*—** A low power (0.4-09V) 2-Bit/Step successive approximation register (SAR) analog to digital converter (ADC) is conferred. A 2-Bit/Step operation technique is proposed which implementing a dynamic threshold configuring comparator instead of number of digital to analog converters (DACs). Area and power is reduced by successively activated comparators. Here the second comparator is activated reflecting the preceding comparator's results. Because the second comparator threshold is configured dynamically for every cycle, only two comparators are required instead of three. By successively activating the comparators, the number of DAC settling is halved, so the power and area overhead is very small and the performance will be increased. The proposed ADC was implemented in a 90nm technology achieved a gain of 35.4 db, power of 0.89 μw and the conversion time of 0.32ns with a supply voltage of 0.4v. The total core area of this ADC is 7.74 μm^2.

Keywords- *SAR ADC, 2-bit/step, low power, threshold configuring comparator.*

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I. INTRODUCTION

Recently, immensely low-voltage circuit designs attract a lot of attention by its supreme power efficiency not only in digital circuits but also in analog circuits. One of the assuring applications of such immensely low-voltage circuits is a wireless sensor network. In the sensor nodes, for easy distribution into the environment, the power must be supplied by using energy harvesting technologies to eliminate the need of a battery replacement. Most of the small size energy harvesting devices can produce extremely low output voltage, for example 0.5 V, and fixed power [1]. Therefore sensor node circuits must operate at immensely low voltage along with low power. Furthermore, the size of the circuits must be as small as possible to slow down the cost of the chip, because massive number of sensor nodes will be embedded in the environment. Therefore we concentrated on designing low-powered analog to digital converters (ADCs) for wireless frontends.

Many low power ADCs for radios and sensor nodes has been suggested, mostly the successive approximation register (SAR) ADC architecture are used [2]-[4]. When compare to other architecture, the SAR ADC produce superior power efficiency. The Other architecture are using power-hungry op-amps. For low speed domains, a number of highly power efficient designs are conferred. By enhancing the charge-redistribution digital-to-analog-converters (DACs) [2] and 500 af unit capacitors are used in the DAC [3], significantly the analog power consumption was minimized. The SAR ADC has high power efficiency at a high resolution can be achieved by designing reconfigurable comparators [4] and bulk voting [5].

While in most of the research, the operating speed is within sensor application and is not adequate for radio requirements which often demand ADCs operating over few tens of MS/s. The SAR ADC has a constriction of speed, because 'n' clock cycles are required for SAR search algorithm, in order to achieve n bit resolution. We have worked on enhancing the speed of low power SAR ADC in the past, the delay time of each cycle will be optimized. However, only the 20% speed is increased. Considering that only the dynamic power are absorbed by the SAR ADC, in order to provide an high speed operation, time interleaving is a better way [7]. Still there is a significant area overhead and timing mismatch calibration circuits makes the system complicated. We can remove the 'n' clock cycle and high speed operation is achieved by using 2-bit/step SAR ADC.

Without time interleaving, the 2-bit/step method [9]-[12] can raise the operating speed. It has attracted care to overcome the speed limits of the SAR ADC.

However, in contrast to the normal SAR ADC, triple times as more elements are needed [9] resulting in a area overhead and large power. In [11], a resistive ladder is used to generate references which absorb dc power. Therefore, designing a power efficient 2-bit/step ADC which can contend with the state-of-the art SAR ADC is challenging.

We suggest a area and power efficient 2-bit/step method. Which is given by adding threshold configuring comparator (TCC) into an normal SAR ADC [8]. By successively activating the comparators, the number of DAC settling is reduced. Even though the power and area is too small, an increase in speed of over 50% can be achieved. By using an

variable current source (VCs) the comparator threshold is configured widely and dynamically. By internally producing voltage the VCs is biased. This maintains the ADC free from varying power supply. A foreground calibration is identified, which needs only a 1/2 V_{DD} input throughout the calibration process. The measured power efficiency is highly comparable with low power state-of-the art works and the operating speed is rapidly increased. Therefore 2-bit/step operation method utilizing TCC has the potential to over the conventional method that generates number of reference voltages.

II. METHODOLOGIES

A. 2-BIT/STEP WITH CONVENTIONAL DESIGNS

The successive approximation search using 2-bit/step method [9]-[12] instead of 1-bit comparator. A 2-bit/step operation method uses a 2-bit quantizer. Because only n/2 cycles are needed for the n-bit conversion, without time interleaving the SAR ADC speed is increased. The little modification is needed in SAR logic to realize the 2-bit/step operation. In the digital circuitry, there will be the small overhead is available. However, providing a 2-bit quantizer need many analog components to be added and the ADC get a area overhead and large power. For example, for the 2-bit quantizer, the flash ADC is the suitable choice. It can collect the comparison results in single clock cycle but has a larger power consumption. In addition, when operating as a 2-bit/step SAR ADC, the reference of the flash ADC should be configured every SA cycle. The reference must be 1/4,2/4,3/4 Vref at the first SA cycle. Before proceeding to the next cycle, the CDAC switches its capacitors then it reflects the comparison results. Therefore the second SA cycle reference is 7/16,8/16,9/16 Vref, respectively. In [9] and [11] too fast 2-bit SAR ADC researches with a different production of references are described.

The 2-bit/step SAR ADC method was first suggested in [9], and in this paper using three capacitor DACs (CDACs) in order to generate the three references. By providing each CDAC different switching codes, three references needed for 2-bit quantizing can be generated for each cycle. The fault of this multi CDAC approach is that the power efficiency drops significantly because analog components are tripled.

When related with 8-bit 1-bit/step SAR ADCs, the analog area and power raise 50% and 200% respectively. In order to relax the power and area overhead, the CDAC was divided to signal DAC and reference DAC, but the area overhead is exponentially raise if further resolution , that is, of over 8 bits, is attempted.

Then again, [11] and [12] use resistive ladder to generate references for the 2-bit quantizer. At every cycle the references are switched as in the fine ADC in subrange ADCs. The references are generated without a lot of power and area overhead, and file the peak power efficiency of 42fJ/conv.at 400 MS/s.

However this result is not proper for low-voltage operation because switches for each reference will need much longer settling. Moreover, the DC current of the resistive ladder will overrule the power consumption at low speed, and lose the power scalability of the SAR ADC.

The preceding researches of a 2-bit/step SAR ADC planned several hundred MS/s to GS/s operation at a standard power supply voltage. Power efficient 2-bit/step for utterly low voltage and low power operation has not been announced yet.

B. 2-BIT/STEP WITH THRESHOLD CONFIGURING COMPARATOR

Rather than using multiple reference voltages, 2-bit/step operation can be implemented by configuring comparator offset (V_{offset}) each cycle. The 2-bit/step SAR ADC enabled with TCC. Here, the CP2 is an normal comparator, which easily analyze the input signal V_{in} and V_{DAC}. Suppose in order that V_{offset} of 1/4 Vref and -1/4 V_{ref} is applied to comparator CP1 and CP3.The comparator threshold (V_{THcomp}) could be3/4 V_{ref} and 1/4 V_{ref}, respectively and 2-bit quantizer is furnished. In this approach, at a certain SA cycle N, V_{offse}t of CP1 and CP3 must be

$$V_{offset} = \pm\frac{1}{2^{2N}} \quad (1)$$

When calibration is completed and V_{offset} is set perfectly. This approach will need only one CDAC and sampling switch, consequently. Hence, power can be extremely minimized when compared with [9] and ADC does not absorb dc power.
However, several area overheads and power remain in this TCC-based 2-bit/step SAR ADC. First, because for each cycle that the comparators should configured their threshold, there is dynamic power of V_{offset} control circuit. Second and most critically, there is an overhead in comparator activation. Although the SA search needs two comparator activation, in 2-bit conversion, the 2-bit flash needs three comparators to be activated. As a result, the comparator power raised 50%. The problem is severe because TCC absorbs large power than ordinary comparator.

C. 2-BIT/STEP WITH SUCCESIVELY ACTIVATED COMPARATORS

For more power reduction, we introduce a 2-bit/step ADC with successively activated comparators (SAC). The block diagram of SAC as shown in fig.1.

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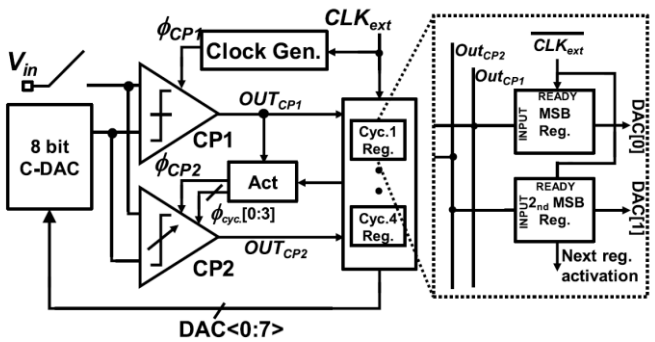

Fig.1 Block Diagram of Proposed 2-bit/step SAR ADC successively activated comparators

The external sampling clock (CLKext) sets down, an SA cycle 1 is started by increasing and φ_1 CP1 determine the first bit (OUT_{CP1}). After the decision of the first bit, V_{THcomp} of CP2 (V_{THCP2}) is set and revert the result of OUT_{CP1}. If the OUT_{CP1} is 1, thus V_{THCP2} is set to 12/16 V_{ref} and the second bit (OUT_{CP2}) is determined. In the proposed ADC, the 2-bit quantizer works like a binary-search ADC [13], so the second comparator is activated reflecting the previous comparator's results. For every cycle the threshold is configured dynamically in the second comparator, only two comparators are needed rather than three. The internal clock generator and register units (cycle N reg) are custom designed logic cells and particular information are discussed in [14]. The results of SA cycle 1 are stored in MSB and 2nd MSB registers, respectively.

A generic SAR ADC cycle time is decided by three delays: SAR logic delay (t_{logic}), comparator delay (t_{comp}), and DAC settling (t_{DAC}). Therefore, the conventional 2-bit/step SAR ADC conversion time is only $4(t_{comp}+t_{logic}+t_{DAC})$, since two bits are processed concurrently. Here the proposed circuit is considered, in this the t_{logic} and t_{DAC} is halved, because the comparators are activated successively [15], there is no enhancement in t_{comp}. Therefore, the conversion time for 8-bit SAC operation is

$$t_{conversion} = 8t_{comp}+4(t_{logic}+t_{comp}) \quad (2)$$

III. DESIGN AND SIMULATION RESULTS

The 2-Bit/Step SAR ADC with SAC was designed and simulated by using Tanner EDA tool and ModelSim. In the Tanner EDA (Electronic Design and Automation) Circuit Design, the low voltage source is given to the circuit for circuit operation. Here the transistors are designed based on the Length and Width. The Length and Width is chosen as L=0.25u W=2.50u and the scaling of these circuit design is fixed as 1. The Circuit Design and Simulation Results are shown below.

A. IMPLEMENTATION OF DYNAMIC COMPARATOR

The Fig. 2 shows the circuit design of dynamic comparator. Here the circuit was designed by cascode current mirror topology. The Regenerative feedback will be used in this comparator. This comparator will increase the speed in ADC.

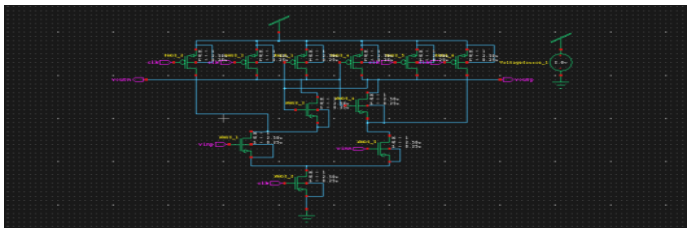

Fig.2 Proposed Dynamic Comparator Circuit

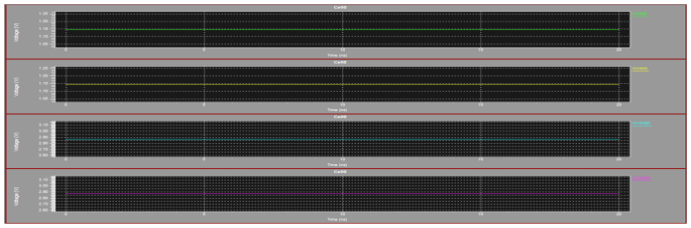

Fig.3 Output of Dynamic Comparator

The Fig.2 and Fig.3 represents the proposed circuit, the given input is only 1.15v and since the comparator operates in the open loop circuit mode so we could see that the output goes to peak value of the supply voltage which is approximately equal to 3V. This clearly shows that it is operating as comparator.

B. IMPLEMENTATION OF 2 STAGE LATCH

The Fig.4 shows the circuit design of 2 Stage latch. It was designed by cascode current mirror topology.

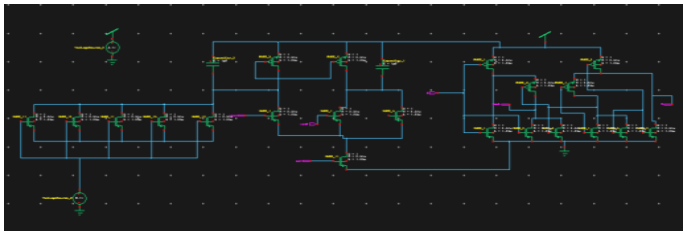

Fig.4 Proposed 2 Stage Latch Circuit

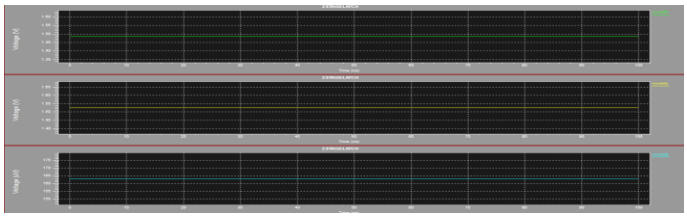

Fig.5 Output of 2 Stage Latch

The Fig.4 and Fig.5 represents the latch samples and retains the value of the input at the positive level of the clock.

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Since the clk=1 so the value in the input 1.55v is being latched to the output which is the addition of sampled output and the latched input.

C. IMPLEMENTATION OF CDAC

The Fig.6 Shows the circuit design of CDAC. This was implemented by cascode current mirror topology.

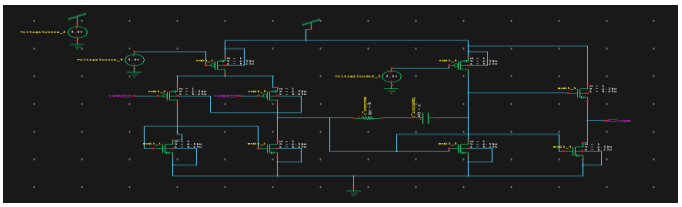

Fig.6 CDAC Circuit

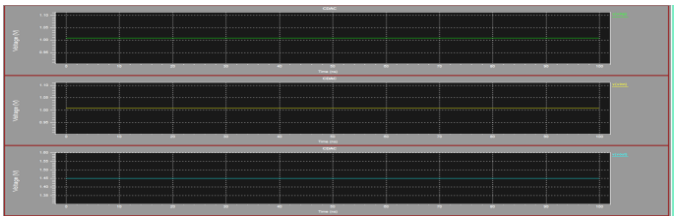

Fig.7 Output of CDAC

The Fig.6 and Fig.7 represents the circuit gives the analog output of 1.1v for the digital input 1v in the circuit it clearly shows that the analog input is obtained.

D. IMPLEMENTATION OF SAMPLE AND HOLD CIRCUIT

The Fig.8 shows the Sample and Hold circuit design. The cascode current mirror topology was implemented.

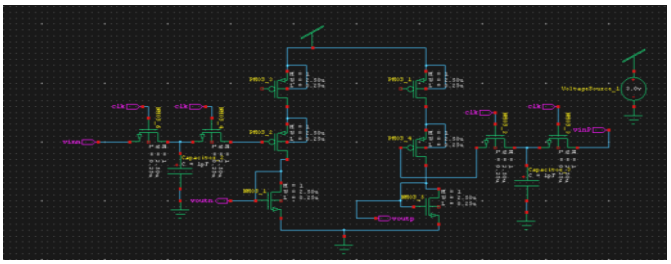

Fig.8 Sample and Hold Circuit

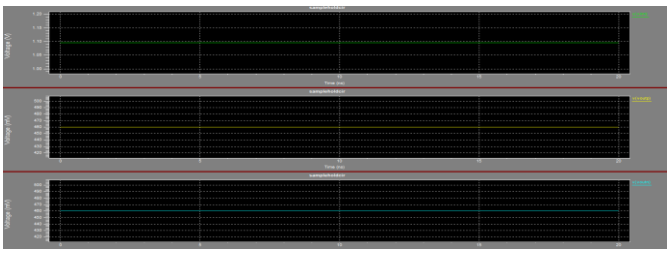

Fig.9 Output of Sample and Hold Circuit

The Fig.8 and Fig.9 represents the sample and hold circuit samples the input and it retains the value in the capacitor even after the sampling period. The input given was 1.1v volt and the S/H circuit holds the value of around 440mv in the circuit even after the sampling in both the nodes at N and P MOS circuit.

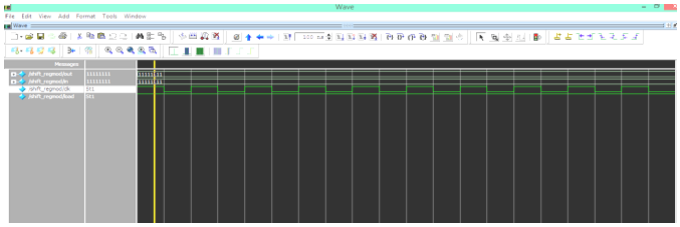

Fig.10 Output of Shift Register

The Fig.10 represents the output waveform of Shift Register by using ModelSim. Here the waveform represents the 8-bit input is given and it will produce the 8bit output and the clock is used to generate the clock pulse internally.

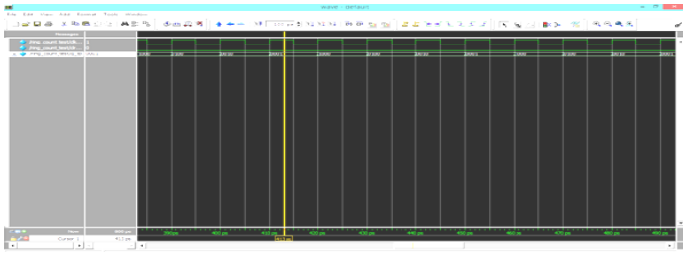

Fig.11 Output of Counter

The Fig.11 shows the output waveform of the counter. This waveform is obtained by using ModelSim tool. In this the counter is used to count the clock pulse. Here the clock pulse will be started in a rising Edge.

TABLE I. Proposed ADC Performance Summary

Technology	90nm TSMC					
Core Area	7.74 μm^2					
Supply Voltage(V)	0.4	0.5	0.6	0.7	0.8	0.9
Power(μw)	0.89	8.23	8.23	78.32	123.6	188.5
Timing(ns)	0.32	0.49	0.49	0.97	1.03	1.18
Gain(dB)	35.4	35.6	35.6	35.9	36.1	36.01

The Table I represents the low voltage of (0.4v-0.9v), and it was achieved the core area, power and timing and gain of these supply voltages. This was implemented in a 90nm technology.

IV. CONCLUSION

An immensely low-voltage operating high-speed and low-power SAR ADC were presented. Using Dynamic threshold configuring comparators, 2-bit/step operation is presented with a small area and low-power consumption. Successive activation of comparators is proposed, It was reduced the more power and its enhanced conversion speed at low supply voltages. The proposed ADC was implemented in a 90nm technology achieved a gain of 35.4 db, power of 0.89 µw and the conversion time of 0.32ns with a supply voltage of 0.4v. The total core area of this ADC is 7.74 μm^2. Further we can reduce even more power and area by implementing in a 32nm technology.

V. REFERENCES

[1] B. H. Calhounet al., "Design considerations for ultra-low energy wireless microsensor nodes, "IEEE Trans. Comput, vol 54, no.6, pp.727-740, june 2005.

[2] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. A. M. Klumperink, and B. Nauta, "A 10-bit charge-redistribution ADC consuming 1.9 µW at 1MS/s,"IEEE J. Solid-State Circuits, vol. 45, no. 5, pp. 1007–1015, May 2010.

[3] A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "A 0.5V 1.1 MS/sec 6.3fJ/conversion-step SAR-ADC with tri-level comparator in 40 nm CMOS," IEEE J. Solid-State Circuits, vol. 47, no. 4, pp. 1022–1030, Apr. 2012.

[4] P. Harpe, Y. Zhang, G. Dolmans, K. Philips, and H. de Groot, "A 7-to-10b 0-to-4MS/s flexible SAR ADC with 6.5-to-16fJ/conversionstep," in IEEE ISSCC Dig. Tech. Papers, Feb. 2012, pp. 472–473.

[5] P. Harpe, E. Cantatore, and A. van Roermund, "A 2.2/2.7fJ/conversionstep 10/12b 40kS/s SAR ADC with data-driven noise reduction," in IEEE ISSCC Dig. Tech. Papers, Feb. 2013, pp. 270–271.

[6] R. Sekimoto, A. Shikata, T. Kuroda, and H. Ishikuro, "A 40nm 50S/s-8MS/s ultra low voltage SAR ADC with timing optimized asynchronous clock generator," in Proc. IEEE ESSCIRC, Sep. 2011, pp. 471–474.

[7] D. Stepanovic and B. Nikolic, "A 2.8GS/s 44.6mW time-interleaved ADC achieving 50.9dB SNDR and 3dB effective resolution bandwidth of 1.5GHz in 65nm CMOS," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2012, pp. 84–85.

[8] K. Yoshioka, A. Shikata, R. Sekimoto, T. Kuroda, and H. Ishikuro, "An 8bit 0.35-0.8V 0.5-30MS/s 2-bit/step SAR ADC with wide range threshold configuring comparator," in Proc. IEEE ESSCIRC, Sep. 2012, pp. 381–384.

[9] Z. Cao, S. Yan, and Y. Li, "A 32 mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13 µm CMOS,"IEEE J. Solid-State Circuits, vol. 44, no. 3, pp. 862–873, Mar. 2009.

[10] H.-K. Hong, W. Kim, S.-J. Park, M. Choi, H.-J. Park, and S.-T. Ryu, "A 7b 1GS/s 7.2mW Nonbinary 2b/cycle SAR ADC with register-to DAC direct control," in Proc. IEEE CICC, Sep. 2012, pp. 1–4.

[11] H. Wei, C.-H. Chan, U.-F. Chio, S.-W. Sin, U.-S. Pan, R. Martins, et al., "A 0.024mm2 8b 400MS/s SAR ADC with 2b/Cycle and Resistive DAC in 65nm CMOS," in IEEE ISSCC Dig. Tech. Papers, Feb. 2011, pp. 188–189.

[12] Y. Lien, "A 4.5-mW 8-b 750-MS/s 2-b/step asynchronous subranged SAR ADC in 28-nm CMOS technology," in IEEE Symp. VLSI Circuits Dig. Tech. Papers, Jun. 2012, pp. 88–89.

[13] G. Van der Plas and B. Verbruggen, "A 150 MS/s 133 uW 7 bit ADC in 90 nm digital CMOS," IEEE J. Solid-State Circuits, vol. 43, no. 12, pp. 2631–2640, Dec. 2008.

[14] A. Shikata, R. Sekimoto, K. Yoshioka, T. Kuroda, and H. Ishikuro, "A 4-10bit, 0.4-1V power supply, power scalable asynchronous SAR-ADC in 40nm-CMOS with wide operating range SAR controller," Trans. IEICE, vol. 96, no. 2, pp. 443–452, Feb. 2013

[15] Akira Shikata, Ryota Sekimoto, Tadahiro Kuroda and Hiroki Ishikuro, "An 8 bit 0.3–0.8 V 0.2–40 MS/s 2-bit/Step SAR ADC With Successively Activated Threshold Configuring Comparators in 40 nm CMOS," IEEE Trans. VLSI Syst., vol. 23, no. 2, pp. 356-368, Feb.2015.

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