

HDL Design $2e^{10}$ -1 Peta Bits Per Second (P.b.p.s) P.R.B.S I.P Core Generator for Ultra High Speed Wireless Communication Products

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Abstract--- The Design is mainly Intended for High Speed Random Frequency Carrier Wave Generator of 1 P.b.p.s Baud Data Rate using $2e^{10}$ -1 Tapped P.R.B.S Pattern Sequence. The P.R.B.S is Designed by using L.F.S.R Linear Feed Back Shift Register & XOR Gate with Specific Tapping Points as per C.C.I.T.T I.T.U Standards. R.T.L Design Architecture Implemented by using V.H.D.L &/ Verilog H.D.L, Programming & Debugging Done by using Spartan III F.P.G.A Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially / Parallel lines I/O.

Keywords: C.C.I.T.T – Consulting Committee for International Telegraph & Telecom , I.T.U – International Telecom Unit, R.T.L- Register Transfer Level, L.F.S.R-Linear Feedback Shift Register, V.H.D.L- Very High Speed Integrated Circuit Hardware Description Language, P.R.B.S-Pseudo Random Binary Sequence. Verilog-Verification Logic

I. INTRODUCTION

In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga/Tera bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing ,wireless Internet Data Packets Transceivers Computing, Tablets,Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers, NOCs, Network-Cards/Racks,Wi-Fi,Gi-Fi, Wimax, G.P.S.G.S.M,Q.C.D.M.ATransceivers. For that purpose ,I Designed Peta Bits Per Second High Speed P.R.B.S is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. P.R.B.S Generators, Receivers, Transceivers Designed for Hi-Fi Wireless Internet Data Packets Computing and Cloud Computing etc.

Transmission, Reception of Data is in the RANDOM Sense, This P.R.B.S Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7,10,15,23,31 at a Clock carrier frequency speed of Gbps/Tbps/Pbps.the Length of PRBS sequence is 2^L-1 . 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, Wi-Fi,Gi-Fi,L.T.E, Wireless O.F.D.M.A , C.D.M.A,Q.C.D.M.A Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms G.b.p.s,T.b.p.s,P.b.p.s . All these P.R.B.S L.F.S.R Sequences are designed by tapping different points according to I.T.U O.150,O.151,O.152 Standards. This P.R.B.S Design Consists of Multiplexer, P.R.B.S Registers of different tapped sequence points, Clock Frequency Generators of Pbps Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using P.R.B.S Checkers. these are simply Linear Polynomial Checkers & C.R.C.

XOR GATE

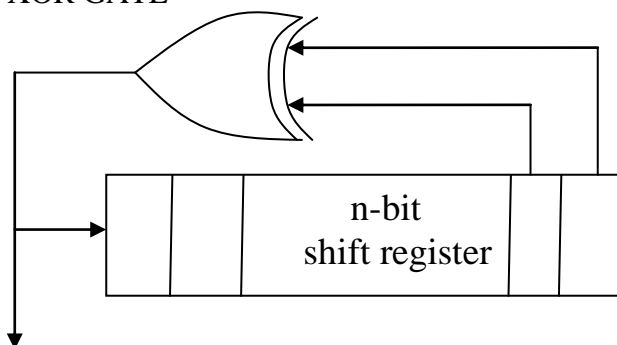
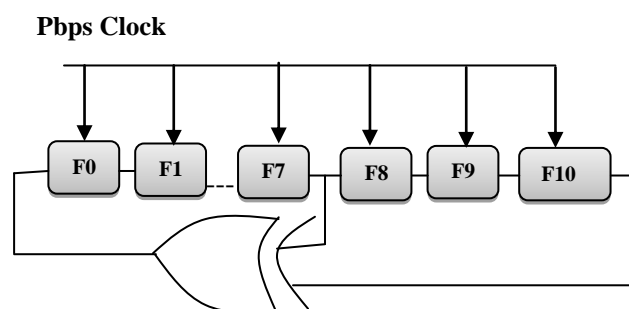


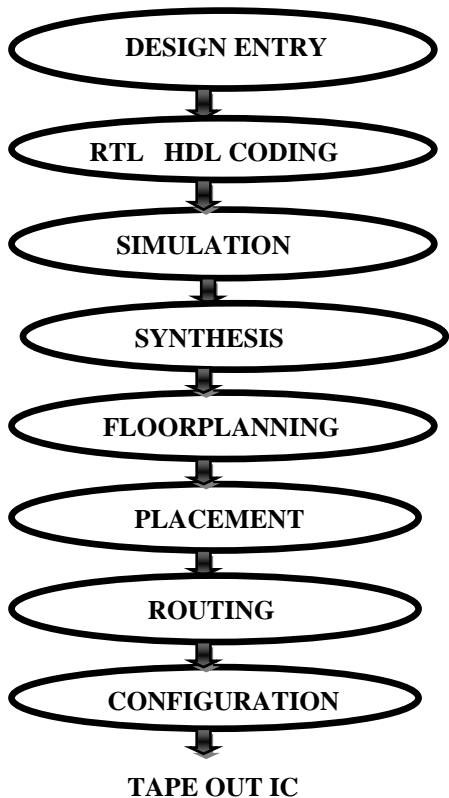
Figure [1]:P.R.B.S DESIGN-Fibonacci (many-to-one)Realization of LFSR with minimum number of taps and XOR gate in its feedback.

3. $2e^{10}$ -1 Peta Bits Per Second P.R.B.S DESIGN ARCHITECTURE



Figure[2]: $2e^{10}$ -1 P.b.p.s Rate P.R.B.S Design

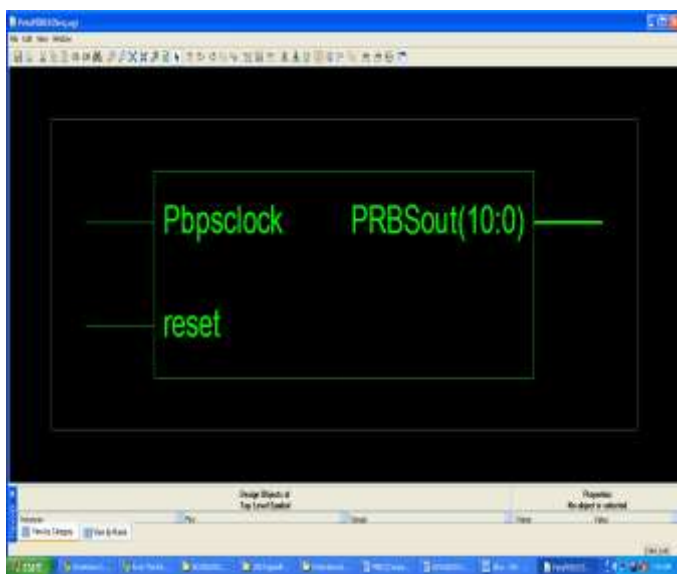
II. SOFTWARE – VLSI IC DESIGN FLOW



Figure[3]: VLSI IC Design Flow Chart

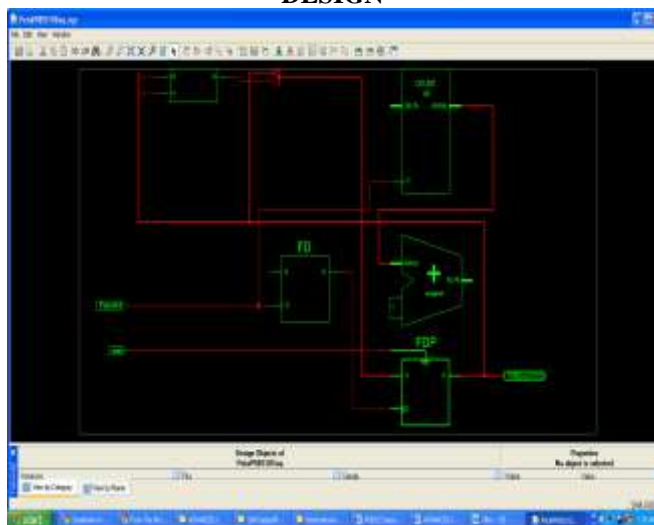
III. DESIGN FLOW REPORTS

A). $2e^{10}$ -1 P.b.p.s Rate PRBS DESIGN RTL BLOCK

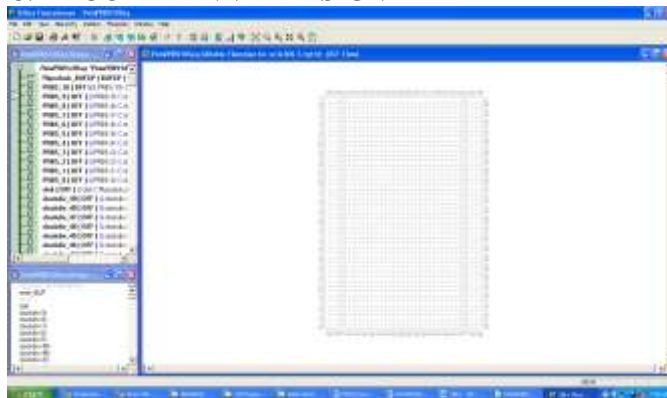


Figure[4]: RTL Design Block $2e^{10}$ -1 P.b.p.s PRBS

B. RTL Schematic- $2e^{10}$ -1 P.b.p.s Rate PRBS DESIGN

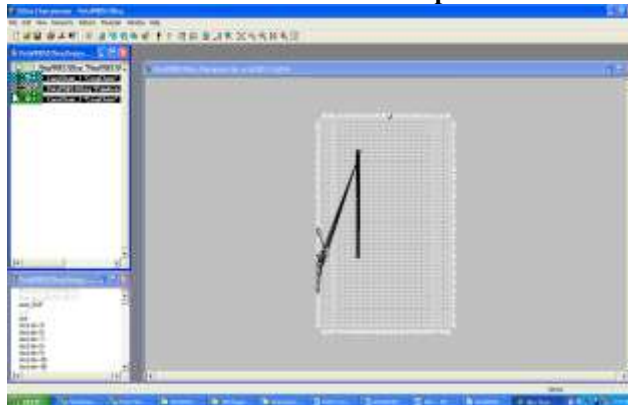


C. FLOOR PLANNER DESIGN



Figure[5]: Floor planner Design $2e^{10}$ -1 P.b.p.s P.R.B.S

C. DESIGN PLACED REPORT –Pbps PRBS



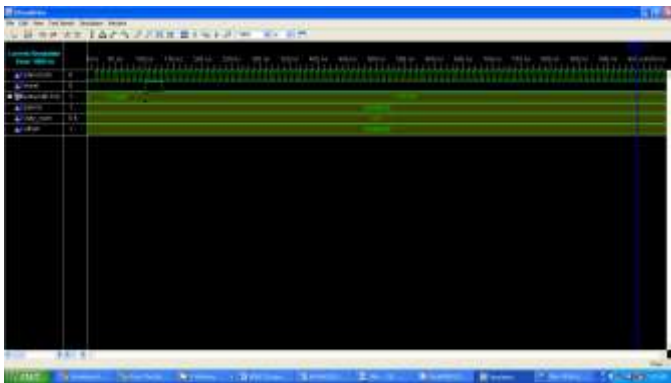
Figure[6]: Placed Design $2e^{10}$ -1 P.b.p.s P.R.B.S

D. DESIGN ROUTED REPORT –P.b.p.s P.R.B.S



Figure[7]: Routed Design Report $2e^{10}$ -1 P.b.p.s P.R.B.S

E. SIMULATION WAVE FORM RESULTS



Figure[7]: Simulation Results- $2e^{10}$ -1 P.b.p.s P.R.B.S
IV. CONCLUSION

Designed High Speed Random Carrier Frequency Generator for Ultra High Speed Wireless Communication Engineering Products

V. REFERENCES

1. http://en.wikipedia.org/wiki/Pseudorandom_binary_sequence
2. ITU – CCITT Reference Document



Prof.P.N.V.M Sastry Currently working with a Capacity of **Dean- IT EDA Software Industry CELL & R&D CELL & ECE DEPARTMENT**, He Did Master Degree In Science- **M.S Electronics**, Under Department Of Sciences, College Of Science & Technology AU -1998. Did PG Diploma In V.L.S.I Design ,I.S.O.U.K.A.S Certified From V3 Logic Pvt Ltd, Bangalore-2001, Did **M.Tech (ECE)** From I.A.S.E Deemed University-2005. Currently Pursuing **(Ph.D)- E.C.E(V.L.S.I)** , **J.N.T.U Hyderabad -2012** , Over **Past 17 years of Rich Professional** Experience with Reputed IT Software Industrial MNC's, Corporate –**CYIENT (INFOTECH)**, **ISiTECH** as a **world top keen IT**

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Dr. D.N. Rao B.Tech,M.E,Ph.D, principal of JBREC, Hyderabad. His carrier spans nearly three decades in the field of teaching, administration,R&D, and other diversified in-depth experience in academics and administration. He has actively involved in organizing various conferences and workshops. He has published over 11 international journal papers out of his research work. He presented more than 15 research papers at various national and international conferences. He is Currently approved reviewer of IASTED International journals and conferences from the year 2006. He is also guiding the projects of PG/Ph.D students of various universities



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