Design of Dynamic Frequency Divider using Negative Differential Resistance Circuit

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Abstract:- The behavior of two frequency divider circuits using negative differential resistance (NDR) circuit is studied. This NDR circuit is made of three resistors (R) and two bipolar-junction-transistor (BJT) devices. It can show the NDR characteristic in its current-voltage curve by suitably designing the resistances. We discuss a dynamic frequency divider, which is made of a R-BJT-NDR circuit, an inductor, and a capacitor. This frequency divider circuit is based on the long-period behavior of the nonlinear NDR circuits generating chaos. It demonstrates the period-adding sequences which appear in its bifurcation diagram to perform the frequency division. We investigate the effects of the input signal frequency on the operation. The results show that the dividing ratio can be selected by changing the input frequency. We also discuss the effect of inputting different types of signals with the same frequency on the operation of this frequency divider. The results show that the input signal distortion has a negligible influence on the frequency divider state.

Keywords:- *dynamic frequency divider, negative differential resistance, chaos, nonlinear circuit*

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I. Introduction

The resonant tunneling diode (RTD) has high potential as functional circuits, which can be developed to many applications [1]-[2], due to the unique negative-differential-resistance (NDR) region in its current-voltage (I-V) characteristic. This device possesses the strong nonlinearity based on the folded I-V curve. A circuit consisting of such nonlinear characteristic often shows the chaos phenomenon. For the past few years, several novel dynamic frequency divider circuits based on the resonant tunneling chaos generator have been developed [3]-[6]. When an external periodic signal is used, such circuit is found to output various kinds of signal waveforms including chaos. The chaos phenomena can be applied widely in the field of communication system [7].

However the fabrication of the RTD device requires the III–V process, such as the molecular-beam-epitaxy (MBE) or metal–organic-chemical-vapor deposition (MOCVD), to implement the circuit. These fabrications are complex and the reproductions are not good because of the quantum-well structure of such device. Therefore, the RTD-based applications are difficult to be compatible with the mainstream ULSI technology including the CMOS and BiCMOS techniques. These processes limit the development of the RTD-based applications

Recently, we have proposed the novel three-terminal NDR devices, which are consisted of standard Si-based metal-oxide-semiconductor field-effect-transistor (MOS) devices and SiGe-based heterojunction-bipolar-transistor (HBT) devices, named as MOS-NDR circuit and MOS-HBT-NDR circuit [8]-[9], respectively. Also, we have developed a simple NDR circuit made of several resistors (R) and bipolar-junction-transistor (BJT) devices. We name this circuit as R-BJT-NDR circuit [10]. These circuits can show the NDR characteristic in their combined I-V curve at room temperature by suitably designing the MOS parameters or resistor values. The major advantage of such NDR circuits is that we can fabricate these circuits using the standard CMOS or BiCMOS process without the need of a MBE or MOCVD equipment.

In this paper, we will design two kinds of chaos generator circuits using the combination of a R-BJT-NDR circuit, an inductor, and a capacitor and demonstrate their applications to the dynamic frequency divider based on a novel operating principle. We investigate the operating margins of this circuit with respect to input signal frequency. In order to discuss the effect of signal distortions, we input three different kinds of signal, such as sine wave, triangular wave, and square wave, to the frequency divider circuits. The results show that the input signal distortion has a negligible influence on the frequency divider state.

II. Characteristics of a R-BJT-NDR Circuit

The R-BJT-NDR circuit is composed of two transistors and three resistors, as shown in Fig. 1(a). During suitably arranging the resistances, we can obtain the NDR characteristic in its I-V curve at the room temperature.

The implement of this NDR circuit is suitable for discrete component or integrated circuit including the CMOS or BiCMOS technology. Compared to the RTD device, the fabrication of such R-BJT-NDR circuit is much easier. Furthermore, this R-BJT-NDR circuit is more convenient to integrate with other active devices and passive devices to

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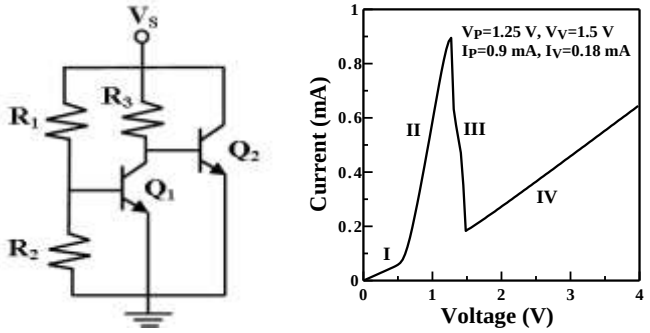
achieve the design of system-on-a-chip (SOC). Figure 1(b) shows the measured I-V characteristic with the parameters designed as R_1=5.5 KΩ, R_2=3.3 KΩ, and R_3=100 KΩ. Both transistors are used the type of 2N3904. As shown, the peak and valley voltages are 1.25 V and 1.5 V, respectively. The corresponding peak and valley currents are 0.9 mA and 0.18 mA, respectively. Therefore, we can obtain the peak-to-valley current ratio (PVCR) is 5.



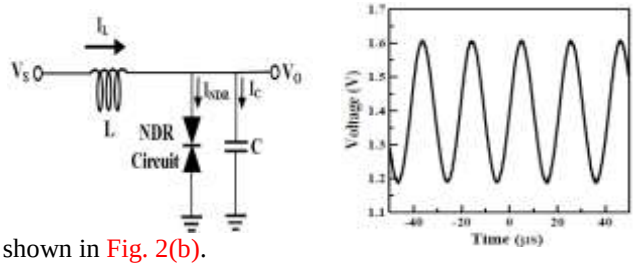
(a) (b)

Fig. 1 (a) Configuration of a R-BJT-NDR circuit. (b) Measured I-V characteristic.

By increasing the input bias V_S gradually, the operation of the I-V characteristic can be divided into four regions as definition in Fig. 1(b). The first segment (I) of the I-V characteristics represents a situation when both Q_1 and Q_2 are cut off. The second segment (II) indicates the case when Q_1 is cut off, but Q_2 is conducted because the V_S is larger than the turn-on voltage of the Q_2 device. The third segment (III) refers to the state when both Q_1 and Q_2 are conducted because the node voltage between R_1 and R_2 is larger than the turn-on voltage of the Q_1 device. Increasing the V_S further, the Q_1 will be saturated and forced the Q_2 is turned off. It will result in the forth segment (IV) of the combined I-V characteristic. The peak voltage is determined by the value of (1+R1/R2)*Von. The parameter Von is the turn-on voltage of the transistor Q_1. If we select different resistor values, we can obtain different NDR I-V characteristics. Hence, this R-BJT-NDR circuit possesses an adjustable I-V characteristic during suitably determining the resistances.

III. NDR-Based Frequency Divider Circuit

The NDR circuit is a strong nonlinear device. The nonlinear system can generate the chaos phenomena where long period characteristic can be obtained in some parameter regions [11]-[12]. This is called the bifurcation phenomena. In the bifurcation region, the output signal period of system will be the integer-multiple of the input signal period. Therefore, we can design a dynamic frequency divider using these period-adding phenomena. Figure 2(a) shows the circuit topology of the frequency divider [4]. This frequency divider consists of a R-BJT-NDR circuit, an inductor, and a capacitor. This circuit is a kind of van der Pol (VDP) oscillator [13]. The VDP oscillator, which is given by a second order differential equation, is a non-conservative oscillator with non-linear damping. The values of the inductor and capacitor are designed as L=100 mH, and C=100 pF here. When a bias 1.4V is applied to this circuit, we can obtain an oscillating waveform with frequency 48.3 KHz and amplitude 0.22 V, as shown in Fig. 2(b).



(a) (b)

Fig. 2 (a) Circuit configuration of a chaos-based frequency divider, (b) Waveform of a van der Pol oscillator.

The periodically forced VDP oscillator provides a periodically disturbed limit cycle that shows a large variety of nonlinear phenomena including mode-locking, period-adding, and chaos. Chaos is often regarded as a random and uncontrollable signal. Basically, the chaos is resulted directly from a loss of stability of a periodic state at a bifurcation point. The well-known route to chaos is the quasi-period phenomenon, where the dynamics of the system initially demonstrate a bifurcation from a stable equilibrium point into periodic oscillation [14]. If the controlled parameter is varied further, continuous bifurcations will make new fundamental frequencies to this system. If these frequencies are incommensurate, we often can observe quasi-period fluctuations from the system. Therefore, we can utilize these characteristics to design a dynamic frequency divider using a chaos-based NDR VDP oscillator. If this circuit is driven by an external periodic signal, we can observe the period-adding phenomena through an alternating period-chaotic transition sequence.

This circuit is driven by an external periodic signal $V_S=V_{DC}+A\sin(2\pi ft)$, with a DC bias V_{DC}, an amplitude A, and a frequency f. Here the V_{DC} is designed at 1.38V which is biased at the NDR region of the R-BJT-NDR circuit, and the amplitude A is fixed at 2V. The frequency f of signal is used as the controlled and modulated parameter. This circuit can output various signal patterns, such as period-adding oscillations and chaos. These phenomena are strongly affected by the circuit parameters and the initial operation conditions. The characteristic frequency, which is defined as $1/(2\pi\sqrt{LC})$, is about 50 KHz for ease of measurements.

When the circuit is operated at the bifurcation region, the output period of the circuit becomes an integer multiple of that of the input signal. If the period of input sine-wave is T, we can obtain the output patterns with 1T, 2T, 3T…and so on under the stable operating conditions. Figure 3 shows the measured input signals and output period-adding oscillation waveforms, where the period is shown from 1T to 8T in order, under different frequencies. The upper and lower parts in each figure are the input signal and output waveform, respectively. These period-adding characteristics mean that the output patterns can be regarded as a dynamic frequency divider.

The operation of the frequency divider can be described as follows. The current passing through the inductor (I_L) is the combined currents of the R-BJT-NDR circuit (I_{NDR}) and capacitor (I_C); $I_L(t)=I_{NDR}(t)+I_C(t)$. The impedance of the inductor and capacitor is proportional and inverse proportional to the frequency, respectively.

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When the input signal is at low frequency, the charges in capacitor are sufficient to switch the NDR circuit during a cycle of the input signal. Therefore, the period of output waveform will be 1T as same as the input signal. However, when the input frequency increases, the impedance of the inductor is increased. The charges supplied to the capacitance are not sufficient to switch the NDR circuit. Therefore, two or more cycles are necessary to switch the NDR circuit. The phenomena are called period-adding bifurcation. Therefore, it we increasing the input signal frequency gradually, the output waveform of this circuit will demonstrate the 1/2, 1/3,…frequency-dividing operation.

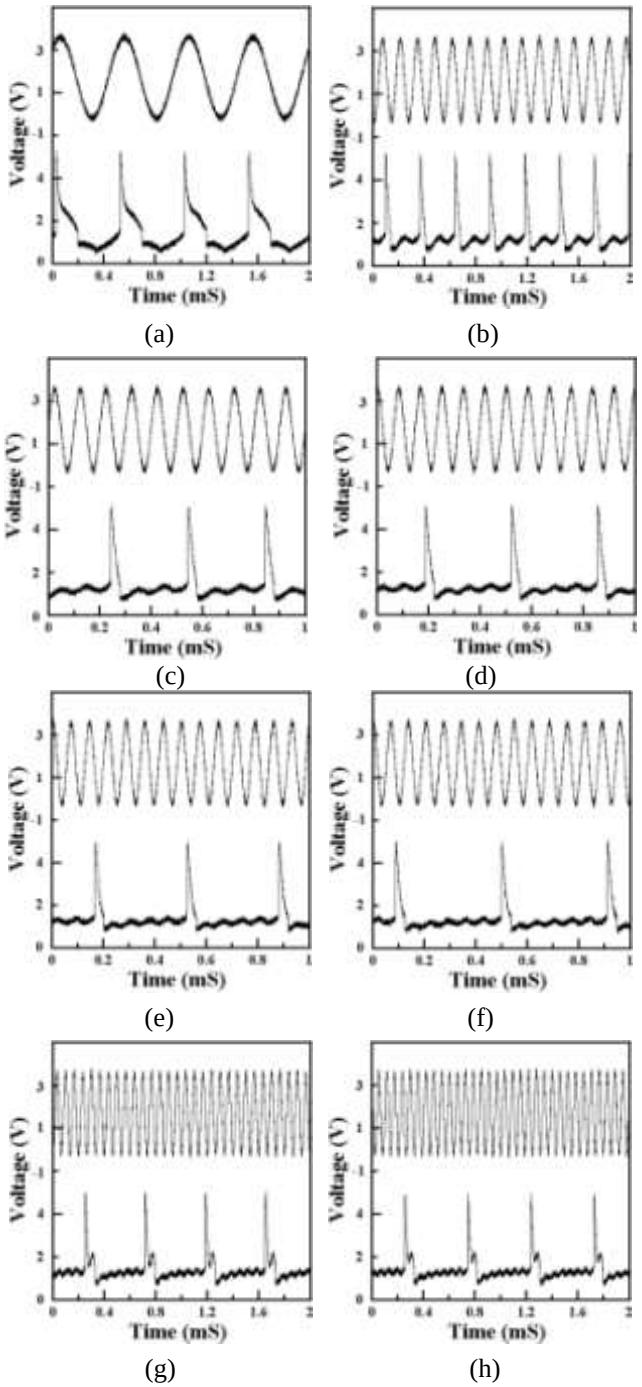

Fig. 3 The output period shows the period-adding oscillation waveforms from 1T (a) to 8T (h) in order by increasing the input frequency gradually.

Based on the measured results, we can obtain the modulation ranges of input signal frequencies with respect to the dividing ratios from 1 to 10 are listed as follows; (1) 0.2 to 5.85, (2) 5.88 to 9, (3) 9.09 to 11.45, (4) 11.48 to 13.23, (5) 13.55 to14.35, (6) 14.4 to 14.86, (7) 14.98 to 15.5, and (8) 16 to 16.9. The unit of frequency is KHz here. The results show that the circuit's output period as a function of the input frequency. Similarly, these dividing ratios can be selected and controlled by the magnitude of input bias or amplitude of input signal. We don't show the results here.

The output period increases discontinuously with increasing frequency gradually, and the chaos regions exist at the transition. Chaos signal means that the signal presents random or quasi-periodic signal. One case of quasi-periodic signal is shown in Fig. 4. The period of output signal is alternately changed between four and five times of that of input signal. After the chaotic transition, the circuit will output periodic stable signal, if we increase the frequency further. Consequently, we can clearly obtain different dividing states using this R-BJT-NDR-based frequency divider circuit under suitable frequency range.

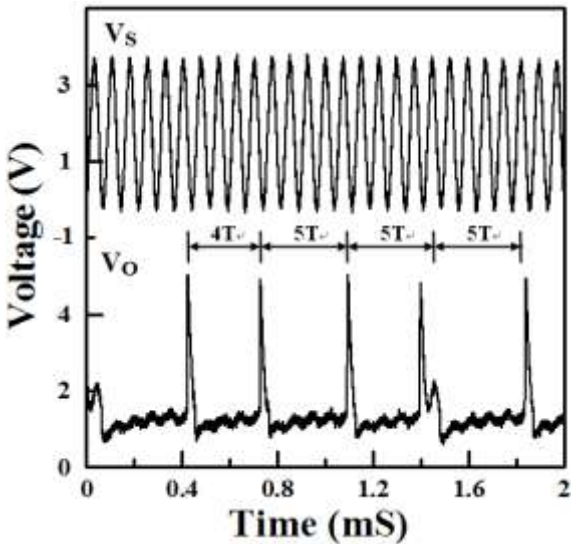

Fig. 4 Measured waveform of V_O in a quasi-periodic condition.

Figure 5(a) shows the other circuit topology of a dynamic frequency divider, which is composed of an R-BJT-NDR circuit in series with the parallel connection of an inductor and a capacitor. The parameters for R-BJT-NDR circuit are the same as that shown in Fig. 1.

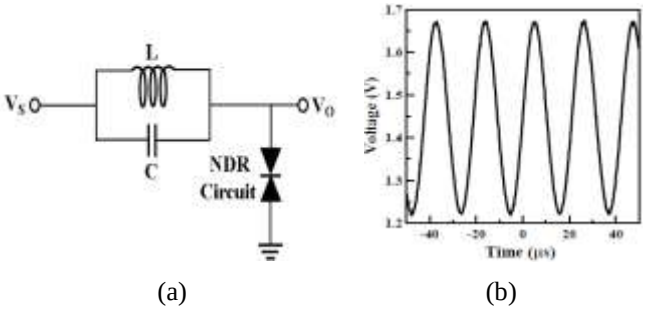

Fig. 5 (a) Circuit configuration of a new chaos-based frequency divider, (b) Oscillating waveform under a bias 1.45V.

This frequency divider is a new configuration which is different from those previously shown [3]-[6]. When this R-BJT-NDR circuit is biased at the NDR region, there is a

parasitic capacitor shunting in parallel with it. This circuit is also a forced VDP oscillator. The values of inductor and capacitor are the same as those previously shown. Figure 5(a) shows an oscillating waveform as we apply a bias 1.45V to this circuit. The frequency is 47.3 KHz with amplitude 0.23 V, as shown in Fig. 5(b).

The current flowing into the NDR circuit is the combined current passing through the inductor and capacitor; that is $I_L(t)+I_C(t)=I_{NDR}(t)$. Similarly, this frequency divider circuit's output period is operated as a function of the input frequency. Figure 6 shows the measured input and output waveforms under different frequency for (a) 1/2, (b) 1/4, (c) 1/6, and (d) 1/8 dividing operations. Parameters of the input signal are the same as those shown in the first one dynamic frequency divider. The results also show that the dividing ratio can be selected by changing the input signal frequency. This frequency divider circuit also can show the other divider ratios, such as 1/1, 1/3, 1/5, and 1/7, which we do not show in the figure. However, we list the modulation ranges of input signal frequencies with respect to the ratios as follows; (1) 0.1 to 5.67, (2) 5.69 to 8.64, (3) 8.7 to 10.88, (4) 10.92 to 12.47, (5) 12.8 to 13.6, (6) 13.65 to 14.05, (7) 14.16 to 14.86, and (8) 14.91 to 15.45. The unit of frequency is KHz here. Compared to the first frequency divider, two circuits have similar ranges for the dividing states. The chaotic phenomena exist between those divided transition region. Those results show that the bifurcation phenomena can be used to implement frequency dividers with a variable dividing ratio.

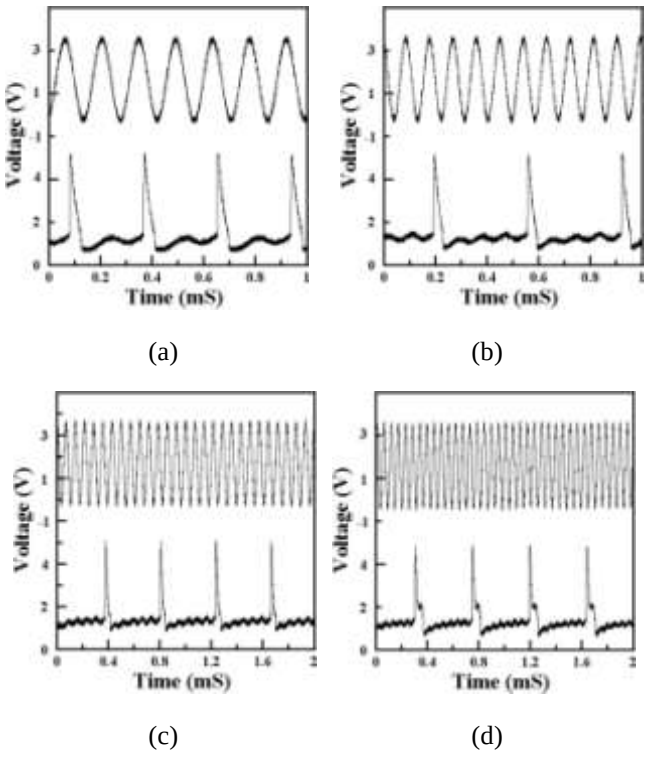

Fig. 6 (a) 1/2, (b) 1/4, (c) 1/6, (d) 1/8, frequency dividing state with respect to input signal frequency.

In order to consider the effect of input signal distortions resulting in the sinusoid signal approaching the triangular and square wave, we input different kinds of signal to the frequency divider circuit. Figure 7 shows the measured results of operation with clear 1/2 dividing states for the first dynamic frequency divider as inputting (a) the sine wave, (b) the triangular wave, and (c) the square wave, respectively. The frequencies are fixed about at 7.8 KHz. The bias V_{DC} and amplitude A is also fixed at 1.38V and 2V, respectively.

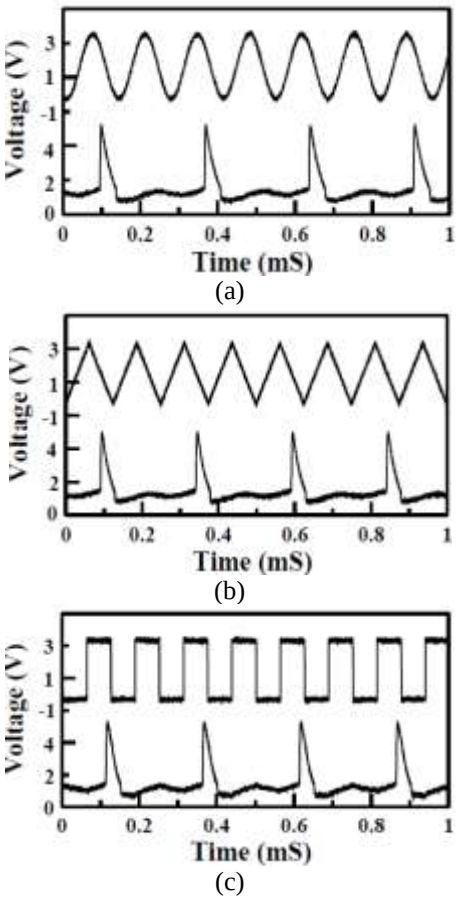

Fig. 7 Measured results for different input signal with (a) sine wave, (b) triangular wave, and (c) square wave. We can obtain clear 1/2 frequency dividing state.

These figures show similar output results in spite of the input signal distortion. It means that the input signal distortion has a negligible influence on the frequency divider state. Also, we find that the modulation ranges for the dividing ratios with respect to input signal frequencies show no noticeable change, as we input different input waveform in this circuit. The similar results can be observed for the second dynamic frequency divider. It means that the input signal distortion has a negligible influence on the frequency divider state.

Because the chaos is sensitively affected by the initial condition of the system, we will observe various output patterns and results by selecting different control parameter. Hence, the amplitude and DC bias of input signal will affect the operation of these dynamic frequency divider circuits. We will discuss their effects on the operation elsewhere.

IV. Conclusions

We have demonstrated two dynamic frequency dividers using the R-BJT-NDR-based chaos circuit. This R-BJT-NDR circuit is made of two BJT devices and three resistors. The modulation of the I-V characteristics and fabrication process of this R-BJT-NDR circuit are easier in comparison with the III-V-based RTD device. This frequency divider is designed using the strong nonlinearity of its NDR characteristic. In

such a nonlinear circuit, its output patterns are changed between chaotic and periodic phenomena strongly depending on the system's parameter. This dynamic frequency dividing operation is based on the bifurcation phenomenon which appears in the waveforms of period-adding oscillation.

We have studied the operation margins of two frequency divider circuits with respect to the frequencies and distortions of input signal. The dividing ratio can be selected by changing the input frequency. The operation regions for two frequency dividers have found to have similar ranges. The measured results also show that the input signal distortion has a negligible influence on the frequency divider state. A higher operating frequency is expected, if the frequency divider is implemented by standard SiGe-based BiCMOS integrated circuit process. Particularly, our NDR circuit is more convenient to integrate with other active and passive devices using the mainstream ULSI technology in comparison with the RTD circuit. These phenomena might provide some useful ideas to design the NDR-based applications.

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