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Efficient Circuit Configuration to Reduce Comparator Requirement of 8-Bit Flash Analog to Digital Convertor

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***Abstract*—** Need constantly exists for converters with higher resolution, faster conversion speed and lower power dissipation. High-speed analog to digital converters (ADC's) have been based on flash architecture, because all comparators sample the analog input voltage simultaneously, this ADC is thus inherently fast. Unfortunately, flash ADC requires 2^N - 1 comparators to convert N bit digital code from an analog sample. This makes flash ADC's unsuitable for high-resolution applications. This paper demonstrates a simple technique to reduce comparator requirement of 8-bit flash ADC that requires as few as 65 comparators for 8-bit conversion. In this approach, the analog input range is partitioned into 64 quantization cells, separated by 63 boundary points. A 6-bit binary code 000000 to 111111 is assigned to each cell. A 8-bit flash converter requires 256 comparators, while proposed technique reduces number of comparator requirements to 65 for 8-bit conversion.

Keywords:- *Flash ADC, µP, DAC, Sample and Hold. Successive Approximation*

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I. INTRODUCTION

Analog-to-digital converters (ADCs) are critical building blocks in a wide range of hardware from radar and electronic warfare systems to multimedia based personal computers and work stations [1]. The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. An N-bit flash architecture uses 2_{N-1} comparators, where N is the stated resolution. Flash converters often include one or two additional comparators to measure overflow conditions [2]. All comparators sample the analog input voltage simultaneously. This ADC is thus inherently fast. The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N, in addition, the separation of adjacent reference voltages grows smaller exponentially, and consequently this architecture requires very large IC's. It has high power dissipation. Two step Flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [3, 4]. However, beyond such resolution, the area and power dissipation of two-step Flash ADC's nearly double for each additional bit of resolution [5]. Typically high-resolution ADC's have been based either on self-calibrated successive approximation [6,7] or over sampling architectures [8, 9]. But both of these architectures are unsuitable for high speed applications. There are many different architectures like pipelined convertor [10, 11], successive approximation convertor [12, 13], Sigma-Delta convertor [14], folding ADC's [15], reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper an 8-bit Architecture of analog-to-digital (ADC) converter is proposed to improve the sampling rate of an ADC. The prototype ADC based on this technique uses only 65 comparators and needs only two comparisons, instead of eight comparisons normally required in the conventional successive approximation techniques for 8-bit resolution. This can increase the speed of conversion.

II. ADC ARCHITECTURE

The block diagram of the proposed 8-bit ADC is illustrated in Figure-1. It is based on a successive approximation technique. The ADC consists of an input sample and hold amplifier (SHA), 6-bit flash ADC, 8-bit DAC, 8-bit µP 8085 and some extra supporting circuit blocks. 6-bit flash ADC partitions input range into 64-quantization cells. From the 6-bit code, µP 8085 decides within which cell the input sample lies. This gives 6 MSB bits 000000 to 111111 according to the cell value. Remaining 2 bits are obtained by successive approximation technique. A binary count is loaded into the Register A depending on the 6-bit code. The detailed binary count to be loaded for different code is summarized in table-I. The Analog to digital converter is designed and developed using µP 8085. The 6-bit code generated by 6-bit flash ADC is fed to Port A of 8255. Depending on the code value, a binary count is loaded in Register A as given in table-I. The successive approximation technique is used to get a final 8-bit digital code for the analog input signal.

III. CIRCUIT IMPLEMENTATION

The block diagram of the 8-bit ADC is as shown in Figure 1. The 8255 port A is used as input port which gets the 6-bit code from Flash ADC. Corresponding 8-bit binary code is loaded into the accumulator as in the table-1. Port B is used as output port, connected to 8-bit DAC to obtain analog signal equivalent to digital count in Register A, which is compared with an analog input voltage V_{IN}. Equivalent 8-bit digital code for analog input signal is obtained by

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successive approximation technique. The conversion algorithm is similar

TABLE I 8-bit count corresponding to 6-bit Flash ADC code

Sl. No.	Output of 6-bit Flash ADC	Count to be loaded in Accumulator
0	000000	00000010
1	000001	00000110
2	000010	00001010
3	000011	00001110
4	000100	00010010
5	000101	00010110
6	000110	00011010
7	000111	00011110
8	001000	00100010
9	001001	00100110
10	001010	00101010
11	001011	00101110
12	001100	00110010
13	001101	00110110
14	001110	00111010
15	001111	00111110
16	010000	01000010
17	010001	01000110
18	010010	01001010
19	010011	01001110
20	010100	01010010
21	010101	01010110
22	010110	01011010
23	010111	01011110
24	011000	01100010
25	011001	01100110
26	011010	01101010
27	011011	01101110
28	011100	01110010
29	011101	01110110
30	011110	01111010
31	011111	01111110
32	100000	10000010
33	100001	10000110
34	100010	10001010
35	100011	10001110
36	100100	10010010
37	100101	10010110
38	100110	10011010
39	100111	10011110
40	101000	10100010
41	101001	10100110
42	101010	10101010
43	101011	10101110
44	101100	10110010
45	101101	10110110
46	101110	10111010
47	101111	10111110
48	110000	11000010
49	110001	11000110
50	110010	11001010
51	110011	11001110
52	110100	11010010
53	110101	11010110
54	110110	11011010
55	110111	11011110
56	111000	11100010
57	111001	11100110
58	111010	11101010
59	111011	11101110
60	111100	11110010
61	111101	11110110
62	111110	11111010
63	111111	11111110

to the binary search algorithm. First, the reference voltage of a particular cell, $V_{ref\ (DAC)}$ provided by DAC is set to $V_N / 2$ to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with $V_N/4$ or $3/4*V_N$ depending on the result of the MSB. If the MSB is "1", then $V_{ref(DAC)} = ¾*V_N$, otherwise $V_{ref(DAC)} = V_N/4$. This sequence will continue until the LSB is obtained. After completion of two comparisons, count in the Register A is digital equivalent of Analog input voltage V_{IN}. To get an 8-bit digital output, 2 comparisons are needed, while it is 8 comparisons in the normal successive approximation ADC. Finally 8-bit digital code is available at port C. Software for implementing successive approximation converter in µP8085 is written in assembler code.

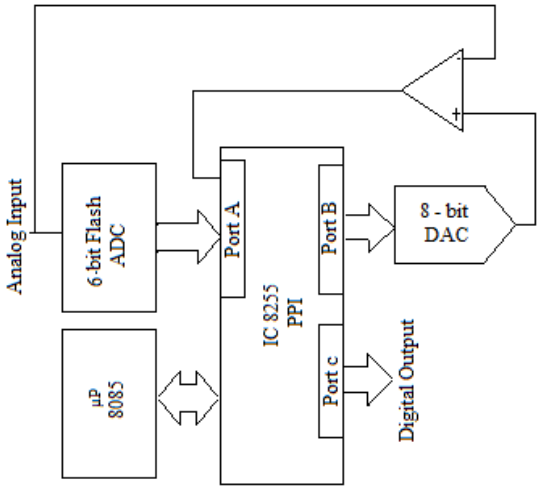

Figure 1. Block Diagram of 8-bit ADC

IV. MEASURED RESULT

An experimental prototype of 8-bit ADC using proposed technique was designed and developed using µP8085. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 3.5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 255 for 8-bit at the output, indicating that the ADC working is functionally correct. Both the differential and integral nonlinearities (DNL and INL) were measured over 2^8 output codes by applying slowly varying full scale range ramp as input to the

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proposed ADC, which completes the full scale range in 255 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a Maximum DNL of 0.49LSB and a maximum INL of 0.48LSB as shown in the Figures 2(a) and 2(b)

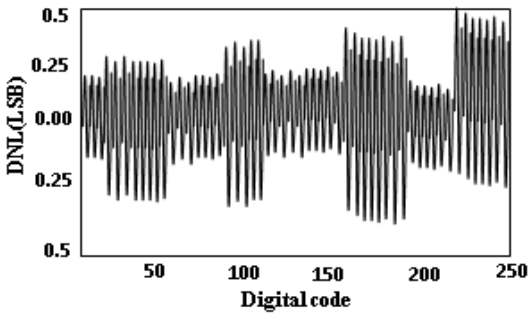

Figure 2(a). DNL Versus output Code

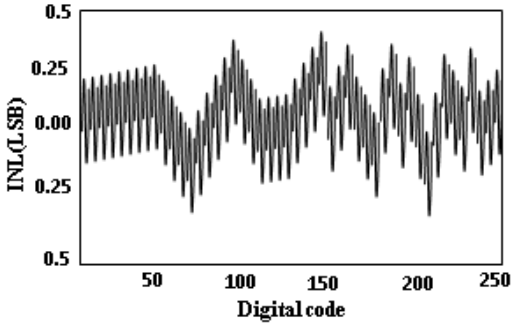

Figure 2(b). INL Versus output Code

V. CONCLUSION

We have presented a simple and effective technique to reduce comparator requirement of 8-bit flash ADC that require as few as 65 comparators for 8-bit conversion. This technique would be effective in a large number of high speed controls and signal processing applications such as hard-disk-drive read Chanel and wireless receivers. Although these applications are most often implemented with Flash convertors, but these ADC's demands larger power. Also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10-bits. This paper shows that partitioning analog input range increases the conversion rate of successive approximation ADC's. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10-bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 10-bit resolution.

Implementation of successive approximation algorithm in Microprocessor has reduced the hardware requirement and cost. Proposed technique uses only 65 comparators to enhance speed of 8-bit successive approximation ADC by 75%.

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