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Efficient Correlator for OFDM Synchronization on FPGA Implementation

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Abstract:-Orthogonal frequency division multiplexing (OFDM) is a viable technology for high-speed data transmission by virtue of its spectral efficiency and robustness to multi-path fading. These advantages can be achieved only with good synchronization both in time and frequency. The existing system consist of pipeline structure of correlator using DSP48E1 slices but it consumes a large amount of area and power and also it introduces a delay. Hence for overcoming these problems we proposed a new model. The proposed model is designed using a custom designed hardware instead of using DSP slices. It reduces area consumption, delay, power consumption and also it can be used in any FPGA architecture.

Index terms *– Correlator, Field programmable gate arrays (FPGA), IEEE 802.16 standards ,Orthogonal frequency division multiplexing (OFDM).*

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I. INTRODUCTION

The Orthogonal Frequency Division Multiplexing technique is used for encoding the digital data on multiple carrier frequencies. For both wired and wireless communication systems OFDM is an very effective modulation technique. OFDM has a spectral efficiency and Robustness for multipath fading. It is specially used for multiple applications in high bit rate wireless transmission system like wireless local area network (WLAN) (802.11) and Metropolitan area network (MAN) (802.16d) [1].

OFDM performance is sensitive to receiver synchronization; carrier frequency offset (CFO) causes inter-carrier interference, and errors in timing synchronization can lead to inter-symbol interference [6]. Therefore, synchronization is critical to the performance of OFDM systems. Many techniques have been proposed for effective OFDM synchronization. The two different transmission modes, continuous mode and burst packet mode, may also require different synchronization schemes [1]. In this paper, we investigate synchronization for burst packet mode, in which all OFDM frames begin with preamble symbols, and both frequency offset estimation and timing synchronization have to be completed within the duration of this preamble. Exploiting the characteristic preamble symbol of two identical halves, Schmidl and Cox [9] introduced metrics for autocorrelation-based synchronization, which can be computed iteratively at low cost and is robust to frequency offset.

Kim and Park [2] proposed a method to improve the robustness of fine STO estimation in the face of large CFO. The method applies multiple cross-correlations with pre-rotation by all possible integer CFOs to calculate fine STO, assuming integer CFO is less than ±6 sub-carrier spacings. However, the method is unsuited to large CFO offsets, and the computational cost is significant since all possible integer CFOs must be calculated.

For implementation on FPGA the autocorrelation related techniques are used due to the low hardware cost. For the implementation of OFDM transceivers the FPGAs, with their highly parallel architecture, are suitable.

In this the timing synchronization is produced by double autocorrelation which is based on short training symbols that allows a reduction in the hardware cost on FPGA system. Fort Comparing the performance and complexity of FPGA implementation of autocorrelation and cross-correlation algorithms. This all results show that the accuracy of cross-correlation algorithms is better than autocorrelation algorithms. While proposing a new cross-correlation implementation is to reduce hardware cost it is still at least five times more complex to implement an autocorrelation, because it requires several multipliers. The Cross-correlation between known preamble and received sample can achieve the highly accurate timing synchronization. However, it requires significant resources. The Multiplierless correlators for timing synchronization were introduced in [3], and designed for IEEE 802.11a OFDM frames which is based on expressing the correlator coefficients as sums of powers of 2 and it require shift and add operations.

For cognitive radios OFDM is one of the main modulation technique, and the FPGAs are an ideal platform owing to their flexibility so, optimizing this the key is only functionality. Modern FPGAs contain different kinds of resources and are used to implement cross-correlation. This all explains the design of several correlators for timing synchronization with preamble symbols based upon IEEE 802.16d. To implement correlation on FPGAs without considering and designing the underlying architecture which results in a highly inefficient implementation. In this all, explains the optimized FPGA designs which is built to fit the FPGA architecture, and also evaluate timing synchronization accuracy, performance resource utilization, and power consumption for understanding when using modern devices whether a multiplier-based mapping is beneficial. The paper divided in five parts which is consist of introduction in section 1, hardware implementation in section 2, implementation result in section 3, simulation and conclusion in section 4 and references in section 5.

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A. Correlator and its type

The correlators are also called as multipliers. It is used in orthogonal frequency division multiplexing. In the 4th generation technology there are multiple person passing multiple data or single person passing several information at the same time. So synchronization problems will occur. For overcome this we are using correlator. wireless communication use the correlator. Correlations are mainly divided as two categories.
(1)Auto correlation: In Autocorrelation containing the same signal but the different parameter used.
(2)Cross correlation: In Cross correlation multiplying two different signal with two different parameter.

II. IMPLEMENTATION OF CORRELATOR

We have to use correlator for reducing the problems of timing synchronization, resource utilization and power consumption in OFDM. The autocorrelation between the received samples is commonly adopted for these synchronizations. As shown in Fig. 1, the downlink preamble of IEEE 802.16d consists of four short training sequences and two long training sequences, each of which follows a cyclic prefix of the corresponding training sequence. The main objective of the repetitive short training sequences is to detect the preamble by performing autocorrelation[8], and the long training sequences are usually used to estimate the fading factors of the channels. To make the auto-correlation independent of the channel environment, the normalized auto-correlation defined below is usually employed.

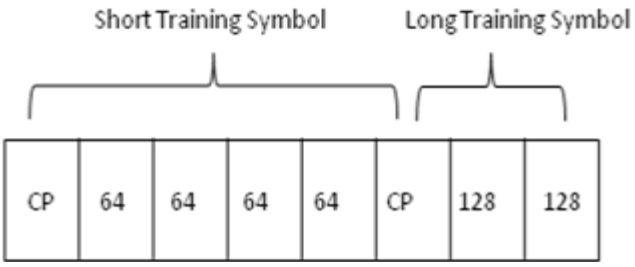

Fig. 1. Downlink preamble symbols for IEEE 802.16.

The 64 samples within the short symbol are used to perform cross correlation with the received samples for timing synchronization. Therefore, the correlators are designed to compare the cross-correlation with 64 constant coefficients of a preamble. From this all description we explore two techniques for implementing the correlators. The first technique based on Xilinx Virtex-6 FPGA DSP48E1 Slices, this is standard approach for an implementation. And Second is the multiplierless correlator which is implemented on each a Xilinx Virtex-6 and a low-power Xilinx Spartan-6 device.
If the both designs implementing without FPGA design then the the synthesis tools would infer the utilization of embedded DSP blocks for multiplication. It takes less timing and unable to optimize the utilization of the DSP block and external logic parts.

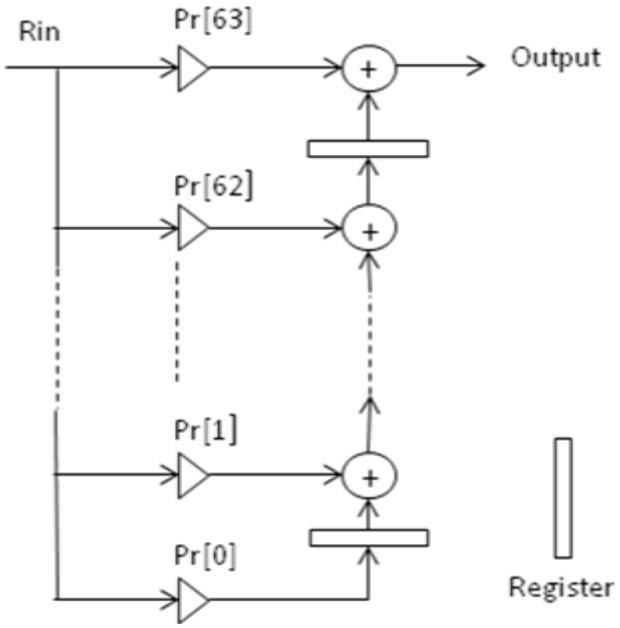

Fig 2: Transpose direct form of the correlator

The DSP48E1 primitives on Xilinx Virtex-6 and later FPGAs are extremely flexible and inside them have an extra circuitry.That permits the design of optimized information methods . However, this should be done manually through writing the code during a particular style. Otherwise, the synthesis tools cannot always infer the most efficient structure. The multiplierless style is given entirely manually as a low-level structural description. The DSP48E1 Slice within the Virtex-6 contains a multiplier factor.

A. Design of Correlator in pipeline structure.

The configurable arithmetic unit which obtained different independent functions, e.g., multiply, multiply-accumulate, multiply-add, three-input add etc. It forms the information path for designing different number of input combinations and register stages. The three stage pipeline have good performance. Fig. 4. Shows pipeline structure of correlator using registers with complex number of multiplier and adder. The first design uses non-pipelined registers in transpose direct type, with 64 coefficients as shown in Fig. 2. The Pr is the preamble corresponding to the sixty four complex conjugated values of samples.
The FIR filter output in transpose direct form is expressed as

$$\text{Output} = Pr[63]Ri + z{-}1(Pr[62]Ri + z{-}1(Pr[61]Ri + \ldots + z{-}1(Pr[0]Ri)\ldots)) \quad (1)$$

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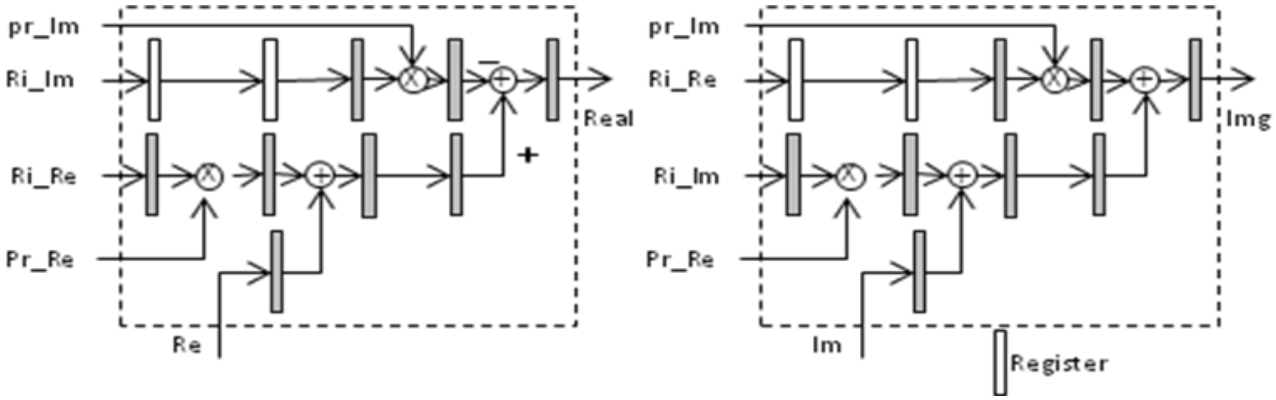

Fig 3: pipeline structure of the complex number of multiplier and adder

The 64 coefficients of preamble are precomputed according to the IEEE 802.16d standard. The above fig 3. Shows pipeline structure of the complex number of multiplier and adder in a five-stage pipeline format which is consisting of registers for three-stage internal pipelining. The Ri_Re and Ri_Im are the real and imaginary elements of received sample. The Pr_Re and Pr_Im are the advanced conjugation of known preamble. The pipeline registers of the Pr_Re, Pr_Im are eliminated because they are considered to be of constant value and Re and Im are the real and imaginary elements of the previous multiplier adder, MAn−1. The output of those complicated multiplier and adder will be expressed as

$$\text{Output} = \text{Ri Pr } z{-}5 + z{-}4 \text{ MAn}{-}1 \qquad (2)$$

Fig. 4 represents the pipeline structure of the correlator using registers and preamble coefficients. The additional registers added in pipeline are needed for handling the received sample. The Addition of pipeline registers should improve the performance considerably.
The output of the pipelined correlator is

$$\begin{aligned}\text{Output} &= \text{Pr}[63]\text{Ri}(z{-}3)63z{-}5 + z{-}4 \times (\text{Pr}[62]\text{Ri}(z{-}3)62z{-}5 \\ &\quad + z{-}4(\text{Pr}[61]\text{Ri}(z{-}3)61z{-}5 + \ldots \\ &\quad + z{-}4(\text{Pr}[0]\text{Ri } z{-}5)\ldots)) \\ &= (z{-}3)63z{-}5\ (\text{Pr}[63]\text{Ri} + z{-}1(\text{Pr}[62]\text{Ri} + \ldots \\ &\quad + z{-}1(\text{Pr}[0]\text{Ri})\ldots)) \qquad (3)\end{aligned}$$

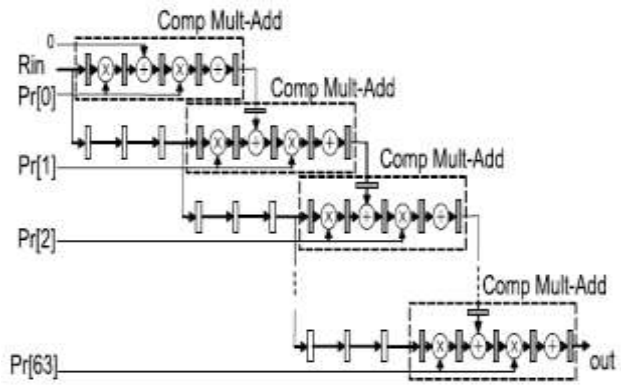

Fig 4: pipeline structure of correlator using resistors

B. Implementation of Multiplierless Correlator

The multiplierless correlators is represents the 64 coefficients of preamble and round them into summed powers of two. So due to the summed power of two we have to performed a shift-and-add operation rather than multiplying by coefficients. It is consider that multiplierless correlation is more efficient than multiplier correlator. However in modern FPGAs with embedded hard multipliers it is not clear whether they should still be considered favorable. Further more, synchronization accuracy should be considered. To expand this, for implementation of four different multiplierless correlators using four coefficient sets with rounding of the increasing degrees, to match the value and performance and evaluation against multiplier-based correlators. The 64 coefficient sets are quantizing the normalized preamble samples with quantizations of 1, 0.5, 0.25, and 0.125. The fig.5 shows multiplierless correlator . This structure based on the transpose-direct form shown in Fig.2.

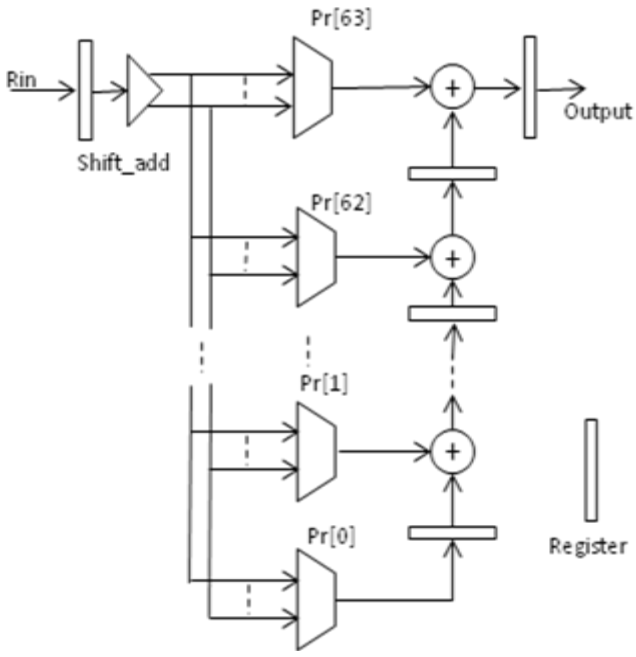

Fig 5 : structure of multiplierless correlator

Instead of using multipliers in which multiply the input samples by coefficients, and in multiplierless correlator the Shift_Add block and multiplexers are used to perform the equivalent operation without an actual multiplication. But the Shift_Add block, multiplexers, and the value of Peamble coefficient are totally different depending upon the quantized coefficient set being used. The Shift_Add block performs shift and add operation on the received samples according to the degree of quantization which is applied on it. To optimize resources of small numbers of bit quantisation, the one common Shift_Add block is used for all sixty four coefficients in place of sixty four separate Shift_Add blocks. This common Shift_Add block calculates all possible values for sixty four coefficients of preamble. The multiplexers are used to select the corresponding values from Shift_Add to accumulate so as to get the correlator output. These are based on the expressed coefficients Pr[n] that are precomputed on the basis of quantizing the sixty four preamble samples. Since the preamble coefficient values are constants, when synthesizing the planning, the electronic device is optimized as hard-wired logic, and the preamble can not be modified. To support totally different OFDM preambles, the Pr[n] may be stored in a register, and a true electronic device used rather than hard-wired logic. This results in increased resource utilization however provides a lot of flexible solution.

III. IMPLEMENTATION RESULT

The Xilinx ISE 13.2, targeting on Xilinx and Spartan-3 (S3) devices were synthesized and completely implemented. The results of design utilization summary that is area unit implementation are according to the quantity of flip flops i.e. taking as registers and four input LUTs(Look Up Table) ,occupied slices and their utilization area unit which is given in Table I. From the table we shows that the number of slices in flip flop available is 3584 out of which 160% is in utilization. That is total 5739 used. However the numer of slice in flipflops available is 7168 out of which 142% is in utilization so total 10224 is used. The number of 4 input LUTs (Look up table) available is 7168 and have the minimum utilization that is 56% hence total number of 4080 used. The total number of bounded input output buffer is 141 and only 35% is in utilization. That is only 50 input output buffer is used. And finally new style has an added necessary advantage is that system used only one global clock buffer therefore share utilization is simply 12%

TABLE I: -FOR MULTIPLIER BASED CORRELATOR

Design utilization summary			
Logic utilization	Used	Available	Utilization
Number of slices	5739	3584	160%
Number of slice flip flops	10224	7168	142%
Number of 4 input LUTs	4080	7168	56%
Number of bounded IOBs	50	141	35%
Number of GCLKs	1	8	12%

IV. SIMULATION AND CONCLUSION

Fig 6: Multiplier based correlator

The fig 6. Shows a simulation of multiplier based correlator. It represents synchronization for IEEE 802.16 OFDM systems. The multiplierless design offers a comparable synchronization performance. The existing system consisting of DSP48E1 slice and it takes higher clock speed. And this is only possible through a pipelined design. Then it takes resource usage and power consumption also greater. So from this above discussion the low power and low cost designs such as Xilinx Spartan-3 do not include sufficient DSP slices. And for low power devices only use multiplierless designs. And one more advantage of multiplierless designs used in any FPGA architecture.

TABLE II:- FOR MULTIPLIERLESS CORRELATOR

Design utilization summary			
Logic utilization	Used	Available	Utilization
Number of slices	528	3584	14%
Number of 4 input LUTs	1056	7168	14%
Number of bounded IOBs	2064	141	1463%

The Xilinx ISE 13.2, targeting on Xilinx and Spartan-3 (S3) devices were synthesized and completely implemented. The results of design utilization summary that is area unit implementation are according to the quantity of flip flops i.e. taking as registers and four input LUTs(Look Up Table) ,occupied slices and their utilization area unit which is given in Table II. From the table we shows that the number of slices in flip flop available is 3584 out of which 14% is in utilization. That is total 528 used. The number of 4 input

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LUTs (Look up table) available is 7168 and have the minimum utilization that is 14% hence total number of 1056 used. The total number of bounded input output buffer is 141 and only 1463% is in utilization. That is only 2064 input output buffer is used.

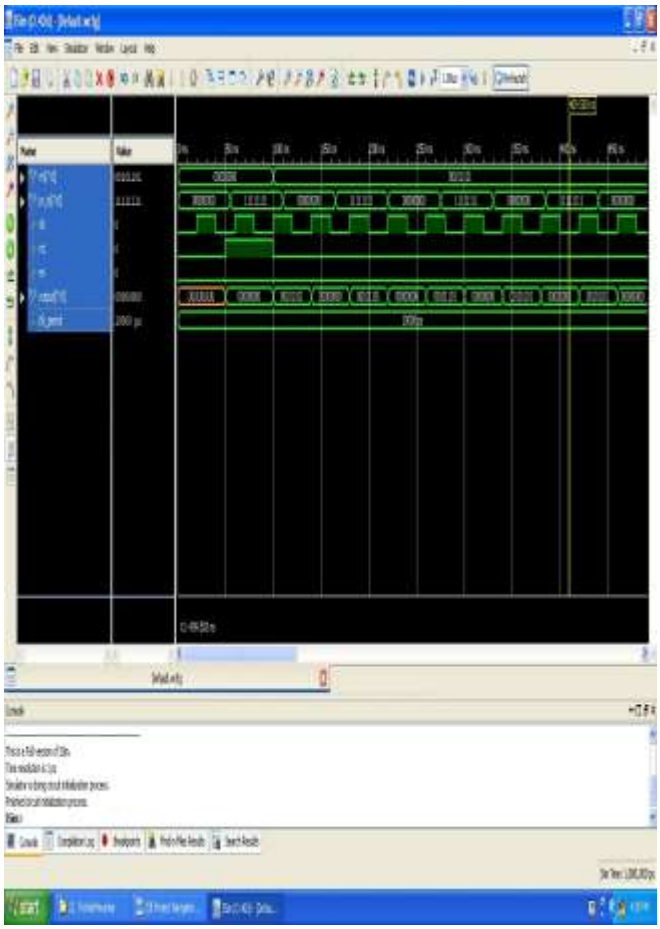

Fig 7: Multiplieless correlator

The fig 7. Shows a simulation of multiplier less correlator. It represents synchronization for IEEE 802.16 OFDM systems. The multiplierless design offers a comparable synchronization performance. . The existing system consist of pipeline structure of correlator using DSP48E1 slices but it consumes a large amount of area and power and also it introduces a delay. Hence for overcoming these problems we proposed a new model. The proposed model is designed using a custom designed hardware instead of using DSP slices. It reduces area consumption, delay, power consumption. And for low power devices mostly use multiplierless designs. And one more advantage of multiplierless designs is it can be used in any FPGA architecture.

While very low quantization resolution does impact on synchronization performance with a quantization step size of input 0.5. The multiplierless correlation on a Spartan-3 can save a 85% power more than DSP slice.

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