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A Hybrid Folded Cascode OP Amp with Positive Feedback and DSB Circuit

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Abstract- A novel high-speed folded-cascode OP Amp with positive feedback and a dynamic switching bias circuit, which increases the speed and lower the power dissipation has been proposed . The proposed Op-Amp was designed in a standard 0.18µm CMOS technology and simulation is performed using tanner EDA tool. Simulation results show a considerable increase in speed, increased output voltage swing and low power consumption for the presented Op-Amp. This proposed circuit overcomes some drawbacks of the conventional circuit in which only positive feedback is used.

Keywords- *Operational amplifier, complementary metal-oxide semiconductor, unity gain band width, dynamic switching bias*

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I. INTRODUCTION

Operational amplifiers (Op-Amps) are one of the fundamental parts of many analog and mixed-signal systems. These are widely used in a wide range of applications from regulators to A/D converters ,D/A converters sample and hold circuits .This fast growth of high speed applications results in a necessary demand to high speed and high gain amplifiers with low power dissipation.

To design high-gain Op-Amps with large bandwidth in low-voltage processes ,always innovative circuit design techniques are required. There are several techniques described in the literature to enhance DC-gain of Op-Amps. One of the conventional approaches to increase DC-gain of folded cascode and telescopic Op-Amps is easily achieved by transistor cascading. Although this approach enhances amplifier output resistance, but leads to limit the output voltage swing . In two-stage Op-Amps, higher DC-gain is achieved by cascading the gain stages. In this method, a proper compensation for stable operation is required. But this compensation will consequently limit the high frequency performance of Op-Amps . Another method which is widely used to enhance DC-gain of Op-Amps is gain-boosting technique . The gain-boosting amplifiers add their own pole and zero to the final Op-Amp and therefore, need a number of external bias voltages and consume more power. Using positive feedback technique is a well-known method to boost the DC-gain of Op-Amps without limiting the high frequency performance . The main problem of the most positive feedback implementation is a strong dependence of the amplifier's gain on transistors matching. Bulk driven methods can also be used for signal amplification in
lowvoltage processes [1]. Higher circuit noise-level is one of the drawbacks of circuits using bulk driven method [1]. In this paper, a new structure is proposed based on the conventional folded cascode Op-Amp shown in figure 2.

Although CMOS Op Amps are suitable for development of filter ICs, the use of several OP Amps results in large power consumption . Accordingly, a simple OP Amp configuration that enables lower power consumption and smaller chip area, even when the number of OP Amps increases, is desirable for large-scale ICs for multi-functional analog processing. In [2]The conventional Op-Amp uses positive feedback technique for increasing the DC-gain of the circuit without affecting the unity gain bandwidth (UGBW), stability, and power dissipation of the circuit. In this paper an improved circuit is proposed by using hybrid of both positive feedback and DSB circuit By using this hybrid technique we can overcome the limitations of [2] i.e speed of the circuit is increased and power consumption get reduced.

DSB CIRCUIT CONFIGURATION:

In Fig. 1, the DSB circuit consisting of M_1-M_4 provides the bias voltage V_B. An external control pulse ϕ_B with a voltage swing of (+1.8 V) drives an inverting switching circuit consisting of the MOSFETs M_1-M_4. When ϕ_B becomes -1.8 V, the OP Amp turns on by setting a bias voltage V_B at an appropriate level by enabling M_3 and M_4 in the saturation region. At this point the op amp turns on and operates normally as an operational amplifier.

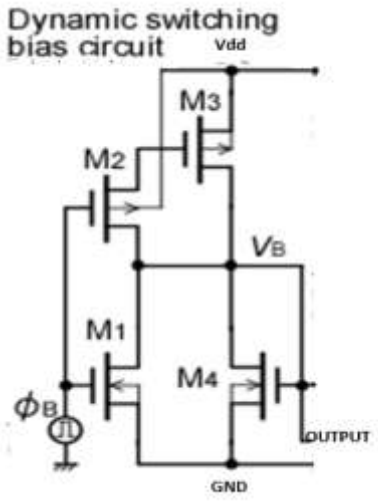

Figure 1: DSB circuit configuration

On the other hand ,When ϕB becomes +1.8V,the op amp turns off by setting VB at nearly -1.8V, enabling M1 to operate in a low impedance and M3 in a high impedance.

Therefore the op amp does not dissipate at all during this off period,thus it is expected that power dissipation become lower.

II. RELATED WORK

[1] In this paper a 0.9V high gain, high speed two-stage Op-Amp is designed and simulated in a 0.18µm CMOS technology. Using both bulk-driven and positive feedback techniques, the dc gain of this Op-Amp is increased about 18.5dB without consuming more power. In addition, the frequency response of the proposed Op-Amp is investigated. Compared to the conventional Op-Amp structure, it is shown that in the proposed Op-Amp, in spite of the decrease of the first pole, the other poles and zeros are not changed. In other words, while the UGBW and phase margin are identical for both conventional and proposed Op-Amps, in the proposed Op-Amp,

[2] In this paper, a novel folded cascode operational amplifier is proposed which improves DC-gain using positive feedback technique. This method does not affect the unity-gain frequency, stability, power dissipation, and output voltage swing of the conventional folded cascode Op-Amp. The proposed Op- Amp was designed in a standard 0.18µm TSMC 1.8V CMOS technology. Simulation results show a DC-gain enhancement of 25dB and 513MHz unity gain bandwidth for the presented Op-Amp. HSPICE simulation results confirm the theoretical estimated improvements.

[3]A new operational amplifier based on the conventional TFC op-amp structure is presented. A novel method is used to increase the dc-gain of the triple folded cascode op-amp. This method does not limit the bandwidth, output voltage swing range and the phase margin of the triple folded cascode op-amp.

[4]in this paper, The implemented design provides a DC gain of around 118 dB with a unity gain frequency of 183 MHz. The design and mixed signal design. With the advancement of process technology, the transistor dimensions are rapidly scaling down leading to reduced ro. In deep sub-micron regime, this leads to a fairly small low frequency gain offered by amplifiers. Applications demanding high gain amplifiers suffer at design level. Even multi-stage architectures fail to provide gain greater than 60 dB. Designers now have to depend on alternate techniques like gain boosting architectures. For most designers designing gain boosting structures using traditional design method become a trivial problem. They often find it difficult to keep all transistors in saturation, particularly in cascode structures. In this work, a simplified design method for designing a fully differential gain boosted folded cascode amplifier is presented. Potential Distribution Method (PDM) guarantees that all transistors is carried out using UMC 180 nm CMOS technology and the simulation results are presented.

[5] This paper presents a high-speed CMOS OP Amp with a dynamic switching bias circuit capable of processing video signals of over 2 MHz with decreased dissipated power. The OP Amp, capable of operating at 10 MHz dynamic switching rate, was designed and showed through simulations a dissipated power of 66 % of that in conventional continuous operation. This OP Amp was applied to a switched capacitor (SC) non-inverting amplifier with a gain of 2and its high-speed 10 MHz dynamic switching operation, capable of processing video signals, was demonstrated. By increasing the switching duty ratio to 70 %, its power dissipation decreased to 56 % of that in normal operation. Some inaccuracy of the SC amplifier resulted mainly from the limited open gain of the OP Amp

[6] this paper presents a 3 stage op amp with a DSB circuit capable of of processing video signals of over 2 MHz with decreased dissipated power. The OP Amp, capable of operating at 10 MHz dynamic switching rate, was designed and showed through simulations a dissipated power of 60 % of that in conventional continuous operation. This OP Amp was applied to a switched capacitor (SC) non-inverting amplifier with a gain of 2and its high-speed 10 MHz dynamic switching operation, capable of processing video signals was demonstrated. Byincreasing the switching duty ratio to 70 %, its power dissipation decreased to 62 % of that in normal operation. Some inaccuracy of the SC amplifier resulted mainly from the limited open gain of the OP Amp was below 1%.this circuit configuration should be very useful in realizing liw power wide bandsignal processing IC.

[7] In this,A high-speed folded-cascode OP Amp with a dynamic switching bias circuit, which enables low power consumption, high gain stably, and a relatively wide dynamic range in low power supply voltages, is proposed. Through simulations, it was shown that the OP Amp is able to operate at a 10 MHz dynamic switching rate and a dissipated power of 71 % of that observed in continuous operation. It also showed an open loop gain of 51 dB and a 0.996 V output dynamic range which is wider than that in a telescopic OP Amp. The 10 MHz high-speed switching operation, allowing processing video signals, was confirmed by applying to a switched capacitor non-inverting amplifier with a gain of below 2. The simulation results showed that the output inaccuracy for a switched capacitor amplifier with a gain of below 2 is below 1.5 %, which is practicable. This inaccuracy was caused by the static nonlinearity of the OP Amp, determined on its limited open loop gain.

III. CONVENTIONAL FOLDED CASCADE OP AMP

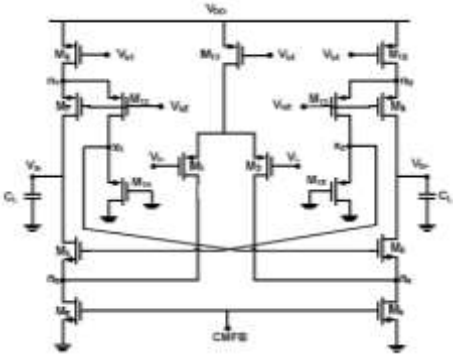

Figure 2:schematic of conventional circuit

Circuit schematic of the conventional Op-Amp is shown in figure 2 . In the conventional circuit, the connection paths between transistors M12 and M13 to the transistors M14 and M15 are connected to the gate of cascode transistors M3 and M4. This is to provide a positive feedback loop inside the Op-Amp

Besides, the CMFB circuitry corrects the offset voltage at the output of the proposed Op-Amp . In this circuit the DC-gain of the conventional folded cascod Op-Amp, has been increased considerably with minimum chosen length for all transistors in a standard 0.18µm CMOS technology. Further to lower the power dissipation and to increase the slew rate of the circuit, a new method based on hybrid of positive feedback and DSB technique has been proposed in section III

IV. PROPOSED FOLDED CASCADE OP AMP

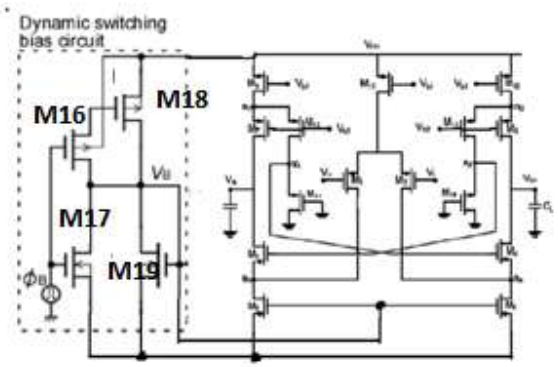

Figure 3:Circuit configuration of the proposed op amp

Fig. 3 shows a configuration of a folded-cascode OP Amp with positive feedback and a dynamic switching bias circuit. The power supply voltages of this circuit are reduced to (±1.8V) of those in the conventional OP Amps for implementing low power dissipation. The DSB method is also used for implementing lower power dissipation.

The op amp operates successfully in a high speed mode.

In this OP Amp, the first stage is the folded cascade stage.A differential input circuit consisting of n-MOSFETs M1,M2 and M11 which increases the dynamic range of folded cascode opamp is used . M5 and load M6 are also turned on/off by controlling a bias voltage of VB switching a DSB circuit dynamically to reduce the power consumption still more**.** In Fig. 3, the DSB circuit consisting of M16-M19 provides the bias voltage VB. An external control pulse VB with avoltage swing of (-1.8 V) (+1.8 V) drives an inverting switching circuit consisting of the MOSFETs M16-M19. When VB becomes -1.8 V, the OP Amp turns on by setting a bias voltage VB at an appropriate level by enabling M18 and M19 to operate in the saturation region, and operates normally as an operational amplifier. Conversely, when VB becomes +1.8 V, the OP Amp turns off by setting VB at nearly -1.8V, enabling M17

to operate in a low impedance and M19 in a high impedance. Therefore, the OP Amp does not dissipate at all during this off period. Thus, it is expected that the power dissipation becomes lower than that in usual continuous operation like the conventional OP Amp

V. CONCLUSION AND RESULT

In this paper a hybrid folded cascade op amp is designed using both the positive feedback and dynamic switching bias circuit. The results are simulated in TSPICE using 0.18µm CMOS technology with a supply voltage of 1.8V . Its characteristics were tested through SPICE simulations. The proposed method increases the speed of the circuit considerably to 598 V/µs which is higher than that of conventional circuit and power consumption is reduced by almost 1.03mW. Also there is a little increase in the output voltage swing..Fig 4 shows the circuit designed in TSPICE

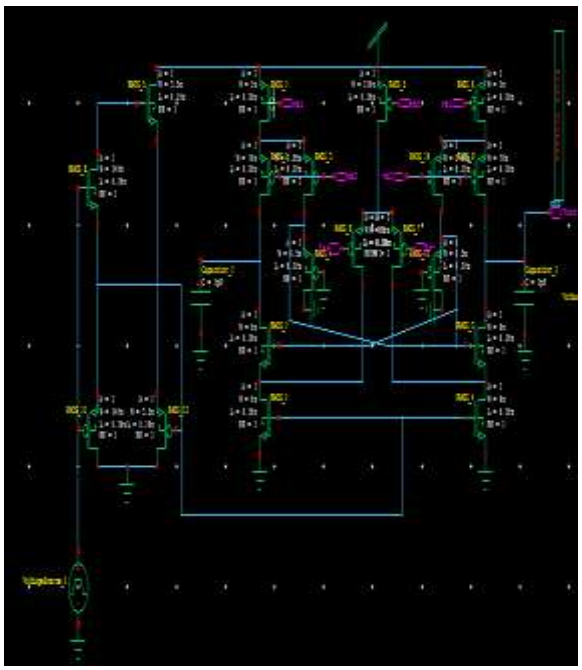

Figure 4:schematic of proposed circuit

Figure 5 shows the simulated waveform which shows the output voltage swing i.e. output saturation voltage having value 1.7 V. further table 1 shows the comparative analysis of various parameters for both conventional and proposed circuit.

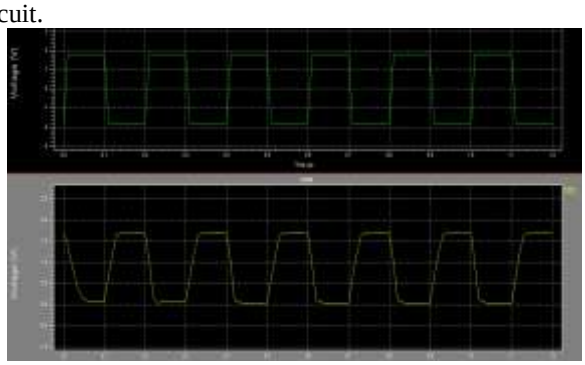

Figure 5: input and output voltage

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TABLE 1 specification of both conventional and proposed op amp

parameter	Conventional op amp	Proposed op amp
Technology used	0.18µm	0.18µm
Supply voltage	1.8V	1.8V
Power dissipation	2.05mW	1.02mW
Slew rate	495V/µs	598V/µs
Output voltage swing	1.550V	1.7V

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