Challenges in Modelling and Verification of Transmitter Circuits for Advanced Mobile Storage Physical layer

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Abstract: Flash memory is a key component of today's mobile phones providing embedded storage for text and media and removable storage for a variety of purposes e.g. Video. Many standard bodies support mobile storage e.g. sdcard.org, Universal flash storage org. Mobile storage today is evolving continuously with ever increasing bandwidth and capacity demands. IP Blocks and Technologies Groups specializes in providing Host controller and Physical Layer solution for variety of mobile devices including phones, tablets, laptops/ultra-books Current project is focusing on Physical layer design and verification – which consists of Digital Frontend (DFE) including Serial/De-serializer, encoding, decoding schemes, and an analog front-end (AFE) which consists of Transmitter/Receiver Circuits. The Phy also includes PLL, Clock Distribution and Compensation circuits to support DFE and AFE. The focus of the current project is to develop methodology and techniques to validate transmitter circuit for mobile storage comprehensively.

Keywords: *Behavior modelling (BMOD), Electrical Rule Check (ERC), PVT (Process Variation and Temperature)*

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1. INTRODUCTION

Rapid increments in handling force, energized by a blend of incorporated circuit scaling furthermore, moves in PC architectures from single- center to future numerous center frameworks, has quickly scaled on-chip total data transmissions into the Tb/s range , requiring a relating increment in the measure of information conveyed between chips as far as possible general framework execution . Because of the constrained I/O pin number in chip bundles and printed circuit board (PCB) wiring requirements, rapid serial connection innovation is utilized for this between chip correspondences.

The two customary routines to build between chip correspondence transfer speed incorporate raising both the per-channel information rate and the I/O number, as anticipated in the current ITRS guide (Figure1). Then again, bundling impediments keep an emotional increment in I/O channel number. This suggests that chip-to-chip information rates must increment significantly in the following decade, showing very much a test considering the constrained force spending plans in processors. While high-performance I/O hardware can influence the innovation changes that empower expanded center execution, sadly the data transfer capacity of the electrical channels utilized for between chip correspondences has not scaled in the same way. Therefore, instead of being innovation constrained, current fast I/O connection plans are getting to be channel constrained. Keeping in mind the end goal to keep scaling information rates, join originators execute modern leveling hardware to adjust for the recurrence subordinate loss of the bandlimited channels.Despite the fact that, with this extra unpredictability comes both force and range expenses, requiring advances in low-control serial I/O plan systems and thought of exchange I/O advances, for example, optical between chip correspondence joins.

There are different types of analog and digital blocks are present in the SOC. The blocks like transmitter, receiver, SerDes, Amplifier, Phase locked loop (PLL), Delay locked loop (DLL), Analog to Digital converter (ADC) and the Digital to Analog converter (DAC) are implemented on the SoC. Figure 1 demonstrates the significant segments of an ordinary high velocity electrical connection framework. Because of the set number of high velocity I/O sticks in chip bundles and printed circuit board (PCB) wiring limitations, a high-data transfer capacity transmitter serializes parallel information for transmission. Differential low-swing flagging is normally utilized for basic mode commotion dismissal and decreased crosstalk because of the natural sign current return way.

At the receiver, the approaching signal is examined, recovered to CMOS values, and deserialized. The high-recurrence clocks which synchronize the information exchange onto the channel are created by a recurrence combination stage bolted circle (PLL) at the transmitter, while at the recipient the examining tickers are adjusted to the approaching information stream by a timing recuperation framework.

2. Objective of the project

To achieve high date rates for the storage, we need high transmitter and receiver's bandwidth (in Gbps) compared to the conventional storage where bandwidth used to be Mbps range. Apart from the bandwidth, one of the challenges is

 ISSN: 2321-8169
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high voltage compatibility of circuits. To support higher voltages (>3V) at platform level, the circuits need to be designed for high voltage tolerance and verified for all reliability issues before the tapeout viz., Electro Static Discharge, Latch-up, Electro-migration, Electrical Overstress and Aging issues. Also as protocols get to higher speeds, it is critical to ensure the circuits integrate seamlessly into the overall datapath (DFE+AFE) between Host controller and external storage device. The focus of the current project is to develop methodology and techniques to validate Transmitter circuit for mobile storage comprehensively.

3. Transmitter

The transmitter must produce a precise voltage swing on the channel while likewise keeping up legitimate yield impedance so as to weaken any channel-incited reflections. Either present or voltage-mode drivers, demonstrated in Figure 2, are suitable yield stages. Flow mode drivers regularly direct momentum near to 20mA between the differential divert lines to dispatch a bipolar voltage swing on the request of ±500mV. Driver yield impedance is kept up through end which is in parallel with the high-impedance current switch. While current-mode drivers are most normally actualized, the force connected with the obliged yield voltage for legitimate transistor yield impedance and the "squandered" current in the parallel end drove fashioners to consider voltage-mode drivers. These drivers utilize a controlled yield stage to supply a settled yield swing on the channel through an arrangement end which is input controlled. While the criticism impedance control is not as basic as parallel end, the voltage-mode drivers can possibly supply an equivalent recipient voltage swing at a quarter of the normal 20mA expense of ebb and flow mode drivers.

4. Generalized description of voltage mode driver and output slew rate problem

Voltage mode and current mode are the two regulating conditions that control the output of the supply. Most applications call for a supply to be used as a voltage source. A voltage source provides a constant output voltage as current is drawn from 0 to full rated current of the supply. In these applications, the power supply runs in voltage mode, maintaining a constant output voltage while providing the required current to the load. A voltage source is generally modeled as providing a lowoutput impedance of the supply.

Voltage-mode logic (VML) drivers are voltage-level perfect with LVPECL. Like CML, these drivers are executed in CMOS, yet have the point of preference that they don't oblige outer pullup resistors, as a result of the utilization of inner NMOS and PMOS transistors to help drive the falling and rising edges. While VML is not yet as generally actualized as the other drivers, regardless it remains voltage-perfect with LVPECL flagging levels and has been utilized as a part of huge numbers of creation gadgets.

The VML drivers that are manufactured as demonstrated in Figure 4. The PMOS and NMOS voltage-controlled voltage sources are utilized to situated VOH and VOL of the driver, and the yield transistor essentially swings between those qualities. The yield swing of VML interfaces is autonomous of the heap impedance.

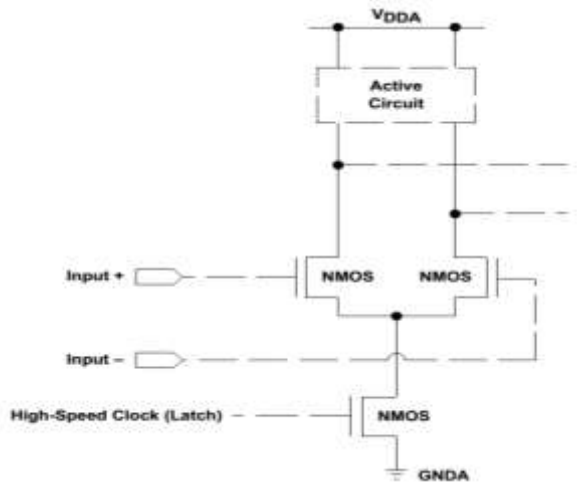

Fig1. Input Stage for Devices Requiring VML Signalling Levels

Output slew rate problem: Sharp slew-rates introduces high-frequency components.EMI issue at the output and reflections from parasitics on the channel. So we need to control the slew rate of the pre-driver.

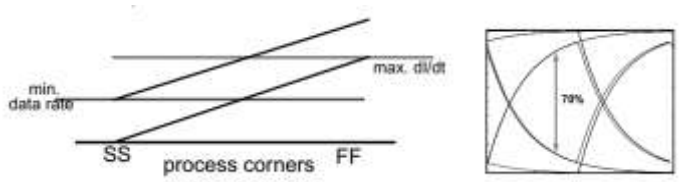

Fig.2.Slew Control

If you compensate for the FF corner the SS corner will become too slow and cause inter-symbol interference of the data.

5. Behavioral Modelling and Emulation

Behavioral Models are representations of analog blocks. We can create analog behavioral models with Verilog AMS or digital behavioral models with System Verilog (and Verilog).

 ISSN: 2321-8169
3813 - 3816

The behavioral models for the following reasons to enable logic validation - The closer our analog modes are to actual analog function, the better our validation coverage, to enable SoC Customer functional validation and to speed up mixed signal design and validation time – Validation can start before design is fully done and can be done at multiple levels of abstraction (bmods, schematic, rtl, etc.

Emulators simply map RTL to underlying hardware to facilitate design simulation at many orders-of-magnitude faster than sw simulators, Emulators help prototype the design to provide a "virtual silicon", helping bridge the gap between RTL and Silicon. This virtual silicon is suitable for running long tests where simulators run out of gas. Emulators enable firmware and software (BIOS) development and testing.Emulators provide an environment where the entire model is run like a SoC.

6. Equivalence check and behavioural modelling

Equivalence check is a subset of formal verification, it is defined as mathematically proving functional equivalency of two representations of a design, one is schematic and other is revised code representing the design. Structural verilog views (cells that instantiate other cells) & custom digital blocks will be FEV'd. It is a requirement that all cells with flops or latches be FEV'd. Matching hierarchy in custom digital blocks is optional. However, it is required that a 1:1 correlation of flops/latches between bmods and schematics remain intact.

7. Electrical Rules Checker

ERC otherwise called Electrical Rule Checks is utilized to weigh for lapses in circuit design. Duet is a principles based quality device by DTS. Duet peruses schematic netlists (printed information) and checks for particular configuration blunders utilizing rules.Performs various types of checks: network, measuring, philosophy requirements, and so forth.

Electrical principles are those properties of a circuit that can be resolved from the geometry and integration without comprehension the conduct. For instance, the evaluated force utilization of a circuit can be controlled by assessing the prerequisites of every gadget and attempting to make sense of what number of the gadgets will be dynamic at one time. From this data, the force conveying lines can be verified whether they have sufficient limit. Notwithstanding power estimation, there are electrical guidelines to distinguish mistaken transistor proportions, shortcircuits, and confined or gravely associated parts of a circuit. Every one of these checks analyze the system and search for irregularities. In this way, while outline tenet checking does sentence structure examination on the format, electrical-guideline checking does punctuation investigation on the system.

8. Simulations

TX with high speed mode

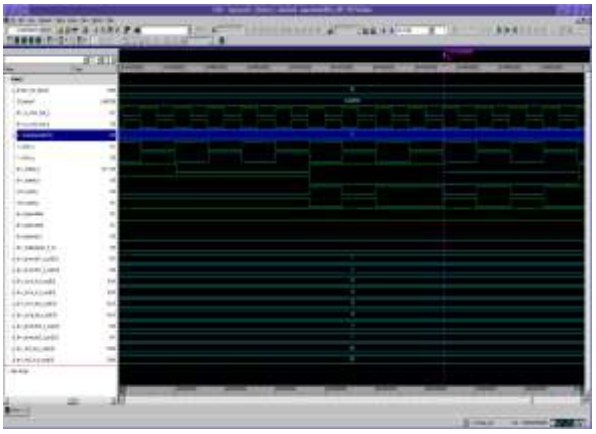

Fig.3. TX with high speed mode

Tx with low speed

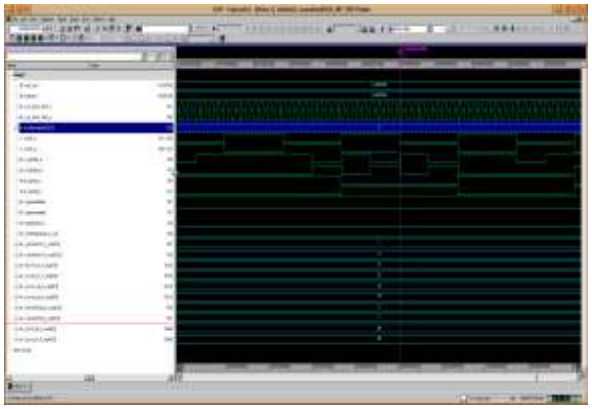

Fig.4. Tx with low speed

9. Conclusion

In the submicron technology as device dimensions becomes smaller and thinner, the criteria for the performance parameter becomes more stringent. Owing to this different kinds of second order effects like short channel effect, narrow channel effect, channel length modulation, punch through, tunneling, mobility degradation, velocity saturation, leakage etc. we have to consider while validating the functional performance of the circuits.
Modelling of analog blocks in digital friendly manner is implemented and tested successfully. Similar test have been made on the models integrating it with the RTL code to give

ISSN: 2321-8169
3813 - 3816

positive results. Formal equivalence check has been done to compare the behavior models with the schematic.

10. References

[1] www.intelpedia.intel.com
[2] www.wikipedia.com
[3] http://www.rulabinsky.com/cavd/text/chap05-4.html
[4] High-Speed Serial I/O Design for Channel-Limited and Power-Constrained Systems, Samuel Palermo Texas A&M University
[5] K.-L. J. Wong et al., "A 27-mW 3.6-Gb/s I/O Transceiver," IEEE Journal of Solid-State Circuits, vol. 39, no. 4, Apr. 2004, pp. 602-612.
[6] J. Poulton et al., "A 14mW 6.25Gb/s Transceiver in 90nm CMOS," IEEE Journal of Solid-State Circuits, vol. 42, no. 12, Dec. 2007, pp. 2745-2757.
[7] R. Payne et al., "A 6.25-Gb/s Binary Transceiver in 0.13-µm CMOS for Serial Data Transmission Across High Loss Legacy Backplane Channels," IEEE Journal of Solid-State Circuits, vol. 40, no. 12, Dec. 2005, pp. 2646-2657.