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Implementation of Power Clock Generation Method for Pass-Transistor Adiabatic Logic 4:1 MUX

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Abstract— we proposed a sinusoidal single phase power clock generation method for 4:1 MUX which is designed in adiabatic logic form. For the power clock generation we presented radio frequency (3 KHz to 3 GHz) DC-AC converter. We have also obtained square wave from RC square wave oscillator consisting of cascaded NOT gates. This square wave and its inverted and phase shifted version are used as gate-drive signals for MOSFET switches those are used in the LC sine wave resonant circuit. The obtained power clock is then applied to a 4:1 MUX which is implemented in Pass-transistor Adiabatic Logic (PAL) style to illustrate power saving. It is observed that PAL 4:1 MUX is about 2 times more power efficient than that of conventional CMOS 4:1 MUX. If for 4:1 MUX, PAL logic is implemented in place of conventional CMOS logic, power saving per MUX that is achieved is about 47%. A 1 µm technology with ml2_20 as library is used for obtaining simulation results.

Keywords *— Adiabatic computing, energy recovery, low power logic.*

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I. INTRODUCTION

Low power dissipation is demand of portable devices to increase battery backup and eliminate difficulties occurred in heat sink design. Amongst several power reduction techniques, adiabatic (energy recovery) logic seems to be efficient. The term 'adiabatic' is originally related to reversible thermodynamic process that occurs without gain or loss of heat and without a change in entropy. In short, it is a process in which there is no exchange of heat with the environment. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity.

Conventional CMOS circuit suffers from CV^2 losses arisen due to abrupt charging-discharging of load capacitances. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than discharging the load capacitors to the ground, so ideally no loss of this energy. This no loss in energy in electrical circuit is similar to no entropy change for thermodynamic system, so the name 'adiabatic'. Conventional CMOS circuits works on DC power supply. Unlike conventional CMOS circuits, adiabatic circuit works on AC power supply. The power supply for the adiabatic operation is usually a trapezoidal or, sinusoidal voltage source. In an adiabatic circuit, there is no need to generate and feed separate clocks to the circuit elements as the AC power supply itself acts as a clock. Hence, the name 'power clock'. A single-phase sinusoidal power-clock can easily be generated using resonant circuits. Here, we present a method of generating AC sinusoidal power clock (PCLK) by using resonant LC circuit. Also PAL 4:1 MUX and conventional CMOS 4:1 MUX were implemented in simulation software and their individual average power Consumption was recorded. Basic parameters, e.g. length and width of MOSFET transistors, are necessarily kept same for both PAL and CMOS MUXs. Comparative study has demonstrated that PAL 4:1 MUX is 2 times more power efficient than conventional CMOS 4:1 MUX.

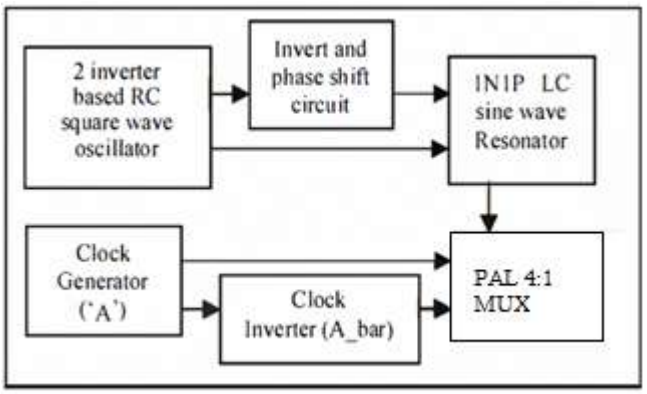

Fig.1. Block diagram of complete system

II. METHODOLOGY

The complete test system is simulated in TANNER EDA S-Edit 13.0 and 1 µm Technology with ml2_20 library was used to obtain the results for both CMOS and PAL circuits. Block diagram of the complete simulated system is as shown in Fig. 1. The first block is 'two inverter based RC square wave oscillator'. It consists of a resistor, a capacitor and two MOSFET inverters those are interconnected together as shown in Fig.2 a. PMOS1 (PM1) and NMOS1 (NM1) together forms first inverter and PM2 and NM2 forms second inverter. Equation 1 gives relation between frequency of oscillation and values of Res 1 (R1) and Cap 1 (C1).

$$f = \frac{1}{R1C1} \quad (1)$$

This circuit oscillates to generate square wave with 10MHz frequency of oscillation and 5V peak voltage. Taking into account internal capacitances of MOSFETS used in inverters, values R1=40K and C1=1pF, causes the circuit to oscillate at 10MHz as shown in Fig. 3(a).

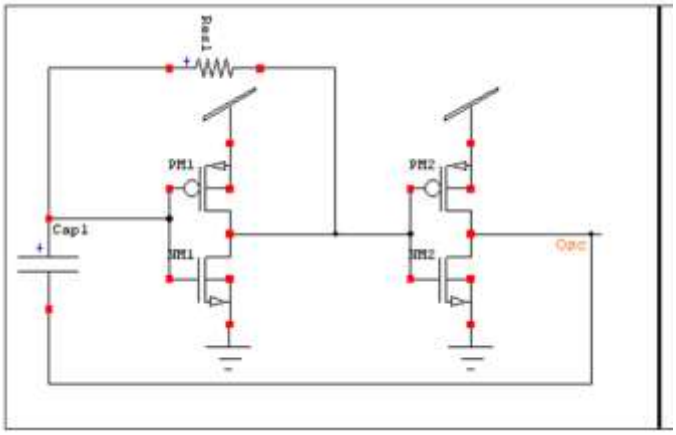

Fig.2 (a) Two Inverter RC Square Oscillator

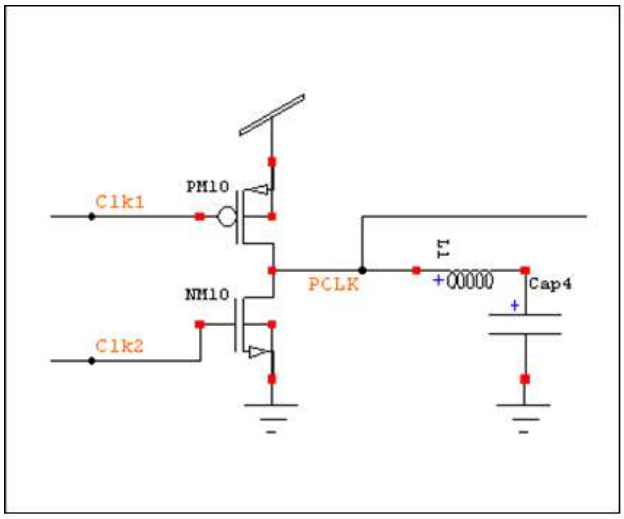

Fig.2 (b) 1N1P LC sine wave Resonator

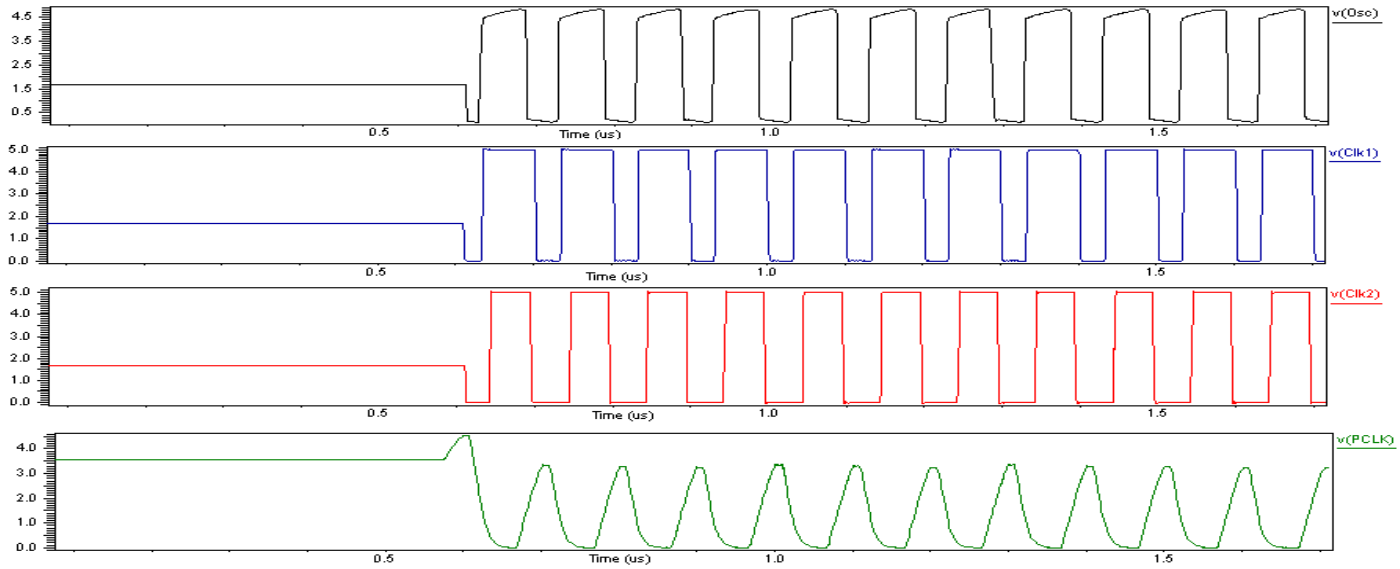

Fig.3. Simulation Results: - (a) V (Osc) is output of Oscillator. (b) V (Clk1) is gate clock for PMOS (PM 10). (c) V (Clk2) is gate clock for NMOS (NM 10). (d) V (PCLK) is Generated Power Clock.

A two-transistor version of the single-phase power clock generator scheme is the 1NIP power clock generator as shown in Fig.2b. 1N1P LC sine-wave Resonator [1] requires two gate drives for MOSFETs, which are inverted and delayed version of each other. Gate drive signals for the two MOSFET switches are as shown in Fig. 4.

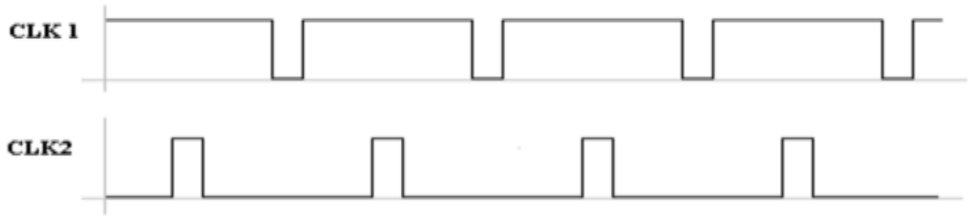

Fig.4 CLK1 and CLK2 gate drive signals for 1N1P single phase power clock generator.

It can be easily observed that CLK2 is inverted and phase shifted version of CLK1. To obtain CLK2 from CLK1, resistor and capacitor together are used as phase shifting (delay) elements and series of CMOS inverters for waveform shaping. In Fig.5 Res2 and Cap2 together in low-pass configuration forms delay element. The square wave fed to this resistor capacitor combination gets delayed as capacitor requires some finite time to charge and discharge depending upon RC time constant. But simultaneously this combination distorts shape of waveform. To restore the shape of waveform, Cascaded inverters are used to get square wave with sufficiently high slew rate. In Fig.3 V (CLK1) and V (CLK2) shows the actual clocks obtained in simulation. As shown in Fig.2 (b) CLK1 is used as gate drive signal for PM10 and CLK2 for NM10. The PMOS is turned on by the gate drive CLK1 at zero voltage, at the peak of the power clock waveform PCLK across the logic. Similarly, the NMOS is turned on by the gate drive CLK2 at VDD voltage, at the valley of PCLK. The large energy-storage capacitor Cap4 stays charged at approximately VDD/2 dc voltage. In [8] this power clock has been described in detail as an ideally lossless gate-drive circuit for MOS power devices. Here, the load is low-energy logic, but the operating principles are the same. By adjusting the device on-off timing, and the device duty ratios, it is possible to obtain a near-trapezoidal power-clock waveform PCLK, which may result in better noise margins and lower losses in the logic.

The 1N1P PCLK generator circuit resonates to generate sine wave [1] with same frequency of 10 MHz but 3.3Vpeak. Reduction in peak voltage is due to critical values of L1 and C4 which are required to get proper shape of sine wave. Resonant frequency is determined by the relation,

$$f = \frac{1}{2\pi\sqrt{L1C4}} \qquad (2)$$

The values of passive elements those are used, are L1=10nH and C4=17pF. The generated PCLK is shown in Fig.3d. Note the inactivity of PCLK for initial 0.6µs. This occurs due to oscillator start-up time. The complete circuit schematic right from oscillator to PCKL generator is as shown in Fig.5.

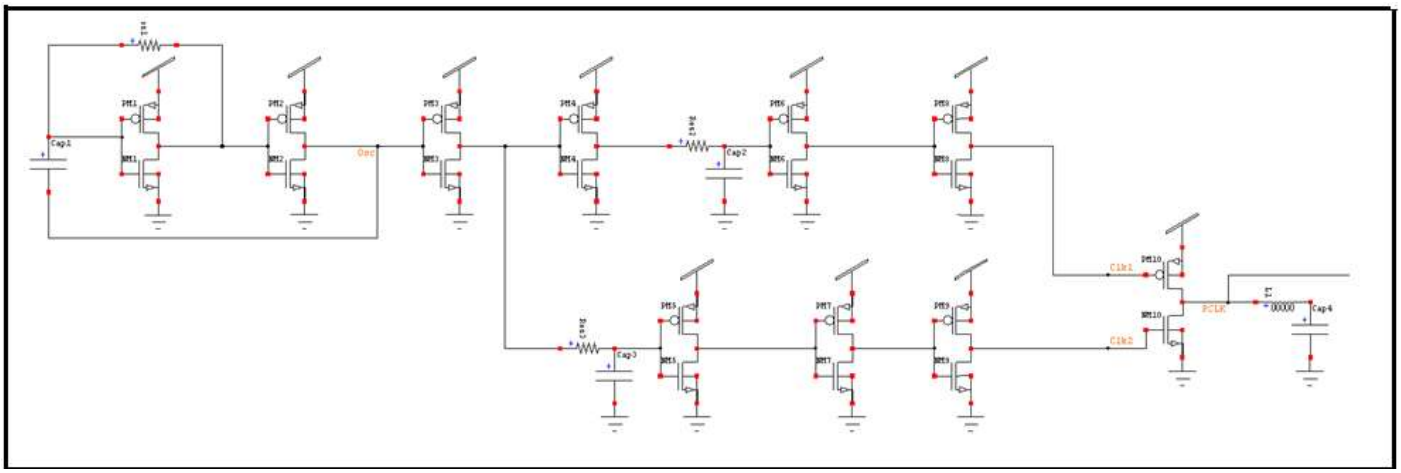

Fig. 5 Complete Schematic of Power Clock Generation circuit

PAL 4:1 MUX, shown in Fig.6 is supplied with the power clock. PAL is a dual-rail logic with pass-transistor

NMOS functional blocks fl and f1_bar, and a pair of cross coupled PMOS devices in each stage, as illustrated by Fig.6, which performs the 4:1 MUX function.

$$f = A.S1.S0 + B.S1.\overline{S0} + C.\overline{S1}.S0 + D.\overline{S1}.\overline{S0} \quad (3)$$

Operation of the gate in Fig. 6 can be summarized as follows: initially PCLK is 0V, and PCLK starts to rise. Suppose that the inputs A, S1 and S0 are high, making a conducting path from the PCLK to the output f1. Given that f1 is connected to PCLK, f1 will start rising from 0V towards the peak of PCLK. The node f1_bar will be "tri-state" and kept close to 0V by the load capacitance of the subsequent gates. As PCLK ramps up, the PMOS1 transistor turns on, and the output is charged up to the peak of PCLK. The transistor PMOS2 will stay off. The power clock will then ramp down toward zero, recovering the energy stored on the node capacitance.

We have kept signal 'A' pulsating with period of 1.6µs and 0.5µs ON time. Here A_bar is inverted version of 'A'. S1 = 3.3V, S0 = 3.3 V and B = C = D = 0V which are kept to be constant. In equation 3, as B = C = D = 0V, the only term that remains is A.S1.S0. As 'S1' and 'S0' are also kept to be logic high, the output 'f' depends only on 'A'. When signal 'A' is high, we get amplitude of PCLK close to 3.3V. When 'A' is low, we get smaller amplitude of PCLK is reduced to about 1.4V. Amplitude of PCLK when signal 'A' is low should be as small as possible. In summary it can be said that waveform of PCLK closely follows signal 'A'. Thus operation of PAL 4:1 MUX is verified.

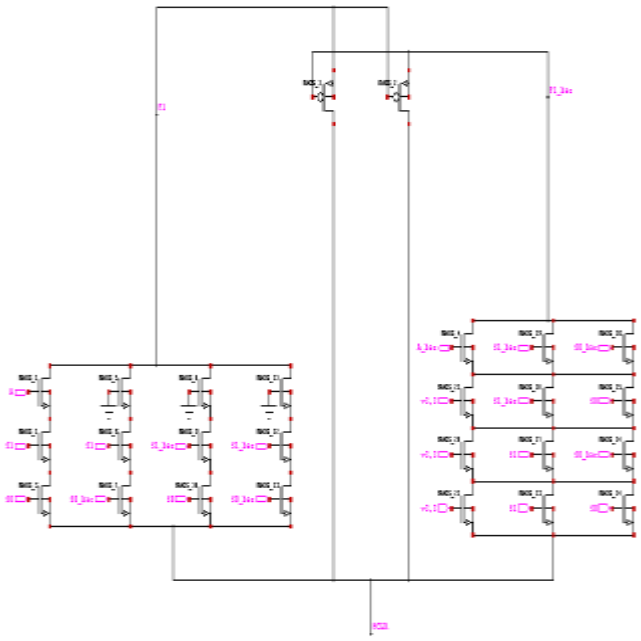

Fig. 6 PAL 4:1 MUX

Fig.7 shows waveforms for SIGNAL 'A', PCLK, f and f_bar.

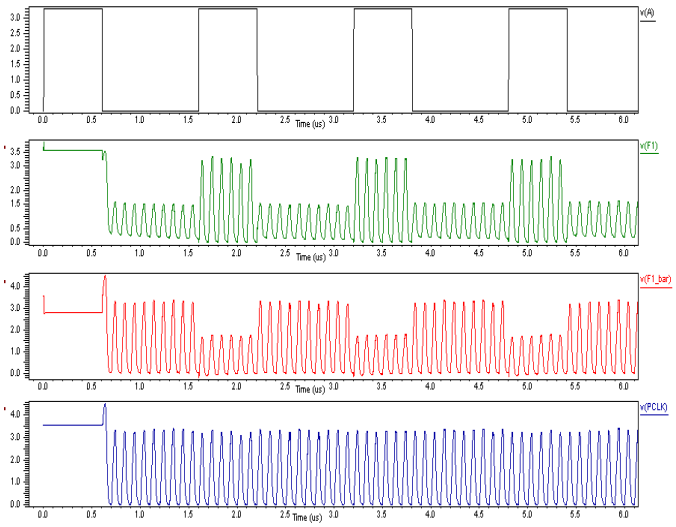

Fig. 7 Simulation Results for Circuit shown in Fig. 6. F1 is the output of PAL 4: I MUX and f1_bar is its complement.

Similarly, we have implemented conventional CMOS 4:1 MUX shown in below Fig. 8 which consisting of 18 PMOS and 18 NMOS. This CMOS circuit is designed from NAND gate MUX design, for designing select line S1 and S0 each NAND gate required one PMOS and one NMOS. For four inputs A, B, C, D each NAND gate requires three PMOS and three NMOS and for output CMOS require four PMOS and four NMOS. All other parameters like length and width of MOSFET transistors, frequency of operation, supply voltages etc are necessarily kept same. So a fair comparison between conventional CMOS and PAL logic styles regarding power dissipation can be made.

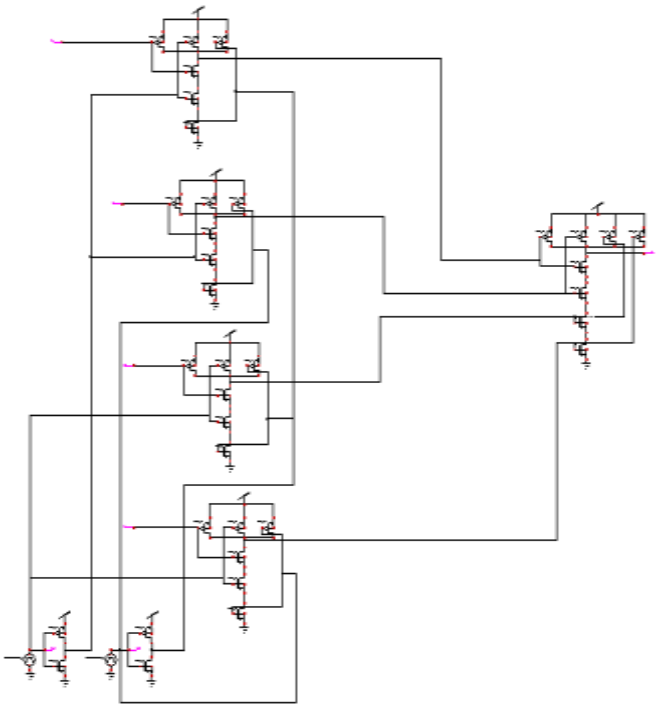

Fig. 8 CMOS 4:1 MUX

Below Fig. 9 show the simulation output for CMOS 4:1 MUX, here S1 and S0 are select lines and A, B, C, D are the four inputs. When S1= 1 and S0= 1 then the output 'Z' is similar to input 'D', when S1= 1, S0= 0 then output 'Z' is similar to input 'C', when S1= 0, S0= 1 then output 'Z' is similar to input 'B', and when S1= 0, S0= 0, then 'Z' is similar to 'A'.

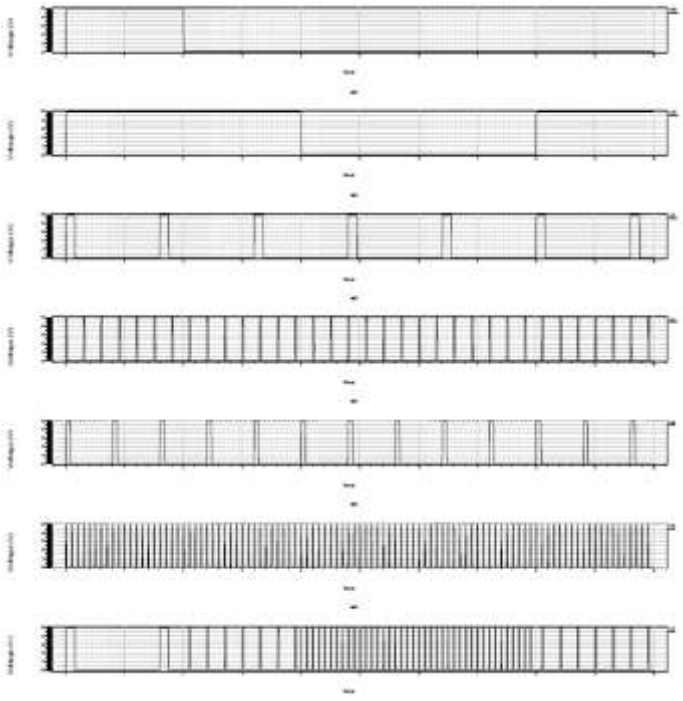

Fig. 9 Simulation output of CMOS 4:1 MUX: 1st and 2nd waves are Select lines S0 and S1 respectively, 3rd, 4th, 5th, and 6th waveform shows inputs D, C, B, A respectively, 7th waveform is output Z.

Here we found out average power dissipation of various blocks separately. Average power dissipated in PAL 4:1 MUX and PCLK generator together is found out. Then subtracting power dissipated in power clock generation (PCLK) from the power dissipated in PAL and PCLK together, we get power dissipated in only PAL 4:1 MUX. Again average power dissipated only in conventional CMOS 4:1 MUX is found out.

RESULTS

For both the logic styles, average power dissipated for various circuits measured from 0µs to 0.1µs time interval are tabulated in Table 1.

Table 1: AVERAGE POWER DISSIPATED IN VARIOUS CIRCUITS

Sr. No.	Power Dissipated	Power (in mW)
1.	PAL 4:1 MUX and PCLK generator together	3.8072
2.	Generation of power clock only	3.7951
3.	Only PAL 4:1 MUX	0.01215
4.	CMOS 4:1 MUX and its Power Supply together	0.02269
5.	Only Power supply of CMOS 4:1 MUX	0.000000025
6.	CMOS 4:1 MUX alone	0.02268

CONCLUSION

Power saving per MUX is obtained by taking difference of power dissipated in CMOS 4:1 MUX with power in PAL 4:1 MUX. Power dissipated in CMOS 4:1 MUX is 0.02268mW and that in PAL 2:1 MUX is 0.01215mW. The net power saving per 4:1 MUX comes to be 0.0105mW. So, about 47% of power per 4:1 MUX is saved if PAL logic is implemented in circuit design instead of conventional CMOS logic. Power dissipated in power clock generation can be considered as penalty because power dissipated in 168 CMOS 4:1MUXs is equivalent to, Power dissipated in power cock generation itself. Ratio of power dissipated in CMOS 4:1 MUX to power dissipated in PAL 4:1 MUX is 2 which signifies that PAL 4:1 MUX is about 2

times more power efficient than conventional CMOS 4:1 MUX.

Table 2: CONCLUSIONS DERIVED FROM TABLE 1

Sr. No.	Description	Value
1.	Power saving per 4: 1 MUX	47%
2.	Power saving per 4: 1 MUX	0.0105mW
3.	Ratio of power in CMOS 4: 1 MUX to power PAL 4:1 MUX	2
4.	Number of CMOS 4:1 MUX required to dissipate the power, as that of power in PCLK generation	168

Keeping aside the increased circuit complexity in PAL implementation, if 47% of power saving per 4:1 MUX is considered then adiabatic logic design seems to be a promising replacement for conventional CMOS circuits in applications demanding very low power dissipation, at low frequency of operation. (up to few hundreds of MHz).

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