Analysis and Design of a Two Stage CMOS OP-AMP with 180nm using Miller Compensation Technique

Shilpa Goyal
M.Tech(Student),
YMCA University of science &
Technology,Faridabad,
Haryana,India,
shilpagoyal30@gmail.com

Nitin Sachdeva
Assistant Professor,
YMCA University of Science &
Technology, Faridabad, Haryana,
India,
n_julka@rediffmail.com

Tarun Sachdeva
Assistant Manager,
Infotel Business Sol. Ltd., Gurgoan,
Haryana, India
sachdeva.t@gmail.com

Abstract: With the continuous growing trend towards the reduced supply voltage and transistor channel length, designing of high performance analog integrated circuits such as operational amplifier in CMOS (complementary metal oxide semiconductor) technology becomes more critical. In this paper the two stage CMOS Operational amplifier (op-amp) has been designed using miller compensation technique which operates at 2.5V. Miller compensation technique has been employed with two approaches, first is using single miller compensation capacitor whereas second approach uses single miller compensation capacitor in series with nulling resistor. To achieve increased phase margin which indicate stability of a system, new design has been proposed with the help of second approach. The simulation was performed using TSMC 180nm CMOS process and design has been carried out in tanner EDA tool.

Keywords: CMOS, Phase margin, Two stage CMOS operational amplifier, Tanner EDA Tool

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I.   INTRODUCTION

In order to achieve higher performance, MOS transistors are scaled down which helps incorporation of more number of transistors on same chip. The continuous growth in processing capacity per chip and operating frequency is result of scaling. Scaling down of CMOS feature sizes enable yet faster speeds, the supply voltage is scaled down to enhance device reliability and improve power consumption. Operational amplifiers are used as a basic building block in many analog and mixed signal systems [1]. During designing of op-amp various electrical characteristics such as gain, offset, phase margin, unity gain bandwidth etc. all have taken into consideration. To meet the desired specification better compensation strategy and topology has to be selected. Among various introduced topologies, here we have chosen up two stage op-amp topology for high input impedance and low output impedance. The first stage provides high gain and second stage provides large output swing. In various op-amp applications, gain with single stage is not sufficient. To achieve higher gain more stages have to be introduced which provides additional phase shift to the system. For Closed loop circuit stability and well maintained magnitude and time response frequency compensation is needed. The important feature of compensation technique is that they can increase the phase margin [4]. The realization of a CMOS op-amp that combines a acceptable gain with high unity gain frequency has been a difficult problem[8].

Operational amplifiers (op-amps) designed o realize different level functioning circuits ranging from simple dc bias generation to high speed signal conditioning or filtering. Operational amplifier can be used efficiently for practical consequences for example switched capacitor designing, analog to digital converters etc.[9].The objective of this paper is to perform a comparative analysis between two stage CMOS op-amp using miller compensation capacitor and two stage CMOS op-amp using compensation capacitor along with nulling resistor effect . Design has been carried out in tanner EDA tool along with simulation results by TSMC 180nm CMOS technology.

II.   TWO STAGE OP-AMP

Operational amplifiers are the integral part in the most analog circuits and systems. Designing amplification block to achieve high gain is not only the concern area for modern op-amp, it also includes proper biasing circuitry along with the effective compensation technique for stable operation. Figure 1 shows the general two stage CMOS operational amplifier (op-amp). It consists of four functional blocks. The first block indicates transconductance stage forms the input of the op-amp followed by the second stage. A common source amplifier generally meets the specification of the second stage. The second stage is mainly used to provide the large output swing with high DC gain for a given supply voltage. Again higher gain leads to lower bandwidth, so designer has to decide between these tradeoffs based on the specifications and the product requirements. Bias circuit is provided to establish the operating point for each transistor in its quiescent stage. The purpose of a compensation circuit is to provide stability to the closed loop performance. Since op-amps are designed to

operate with negative feedback connection so frequency compensation is necessary for stability. The feed forward path through miller capacitor introduces a right half plane (RHP) zero which degrades the phase margin of the system. However, the RHP zero can be eliminated by using the nulling resister in series the compensation capacitor [10].
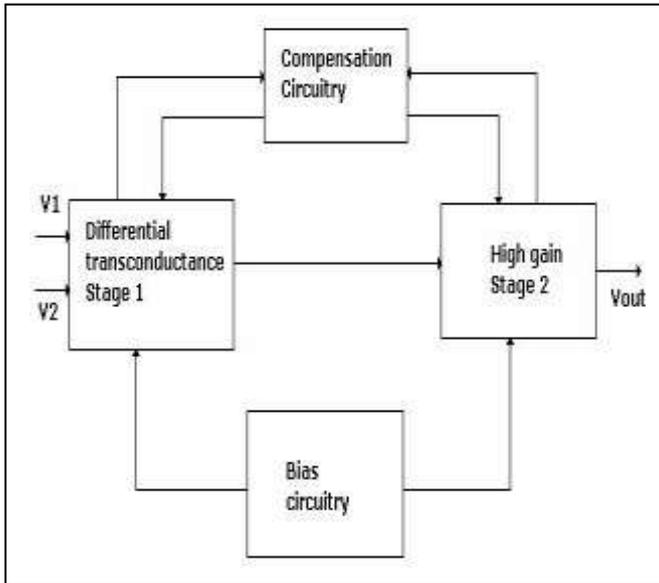

Figure 1. General Structure of Two Stage CMOS op-amp

This op-amp architecture has many advantages: high open-loop voltage gain, rail-to-rail output swing, large common-mode input range, only one frequency compensation capacitor, and a small number of transistors. This operational amplifier structure has wide usage in various analog circuits and systems applications.

The topology used for two stage CMOS op-amp is shown in figure 2. The circuit consist of 8 transistors out of those 5 are NMOS and remaining 3 are PMOS transistors. The transistors named from M1 to M4 are showing the differential transconductance first stage of the circuit. The M1 and M2 are the N-channel MOSFET transistors forming the input stage to the op-amp circuit. The current mirror configuration comprised of M3 and M4 used as a active load for input differential stage. Second stage uses current sink load inverter where M6 acts as driver and M7 works as load. The output from drain of M2 will be amplified using current source configuration represented by M6. The biasing in a circuit is achieved using two transistors M5 and M8 and a current source. The compensation capacitor is shown by C_C and the load capacitor is represented by C_L.
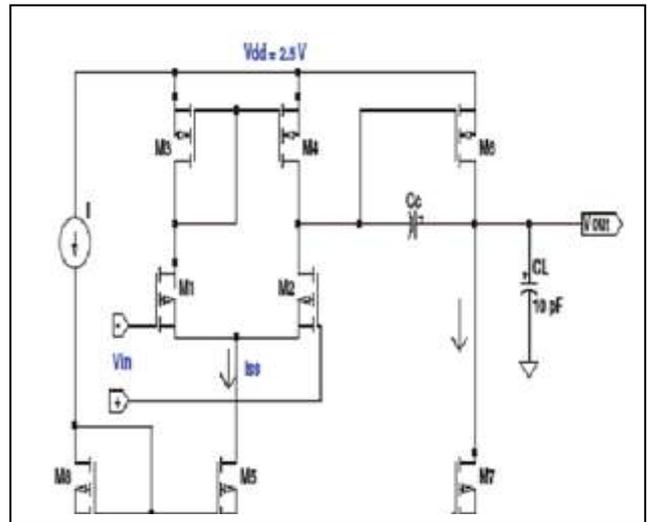

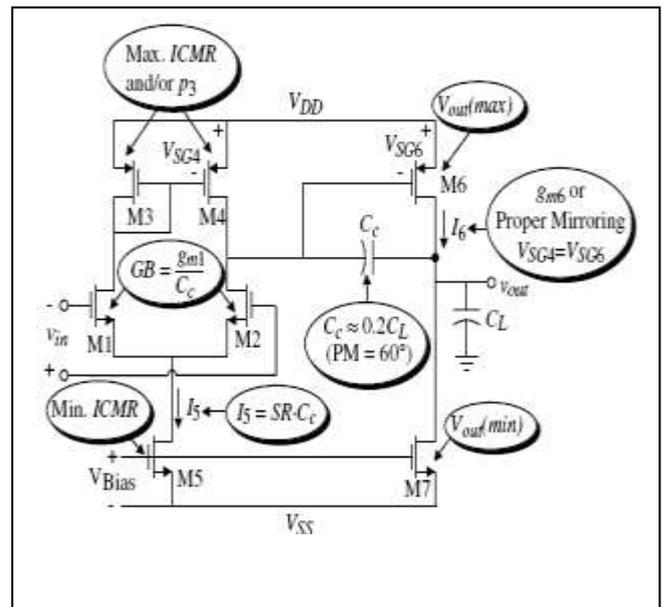Figure 2: Topology Used for Two Stage CMOS op-amp

Figure 3. Illustration of a Design of Two Stage CMOS op-amp

III. TWO STAGE CMOS OP-AMP WITH COMPENSATION STRATEGY

The schematic for unbuffered two stage CMOS op-amp with single capacitor miller compensation (SCMC) is represented in figure 4. It is considered that all MOS transistors are operating in saturation region.

TABLE 1. Specifications for Two Stage op-amp Design

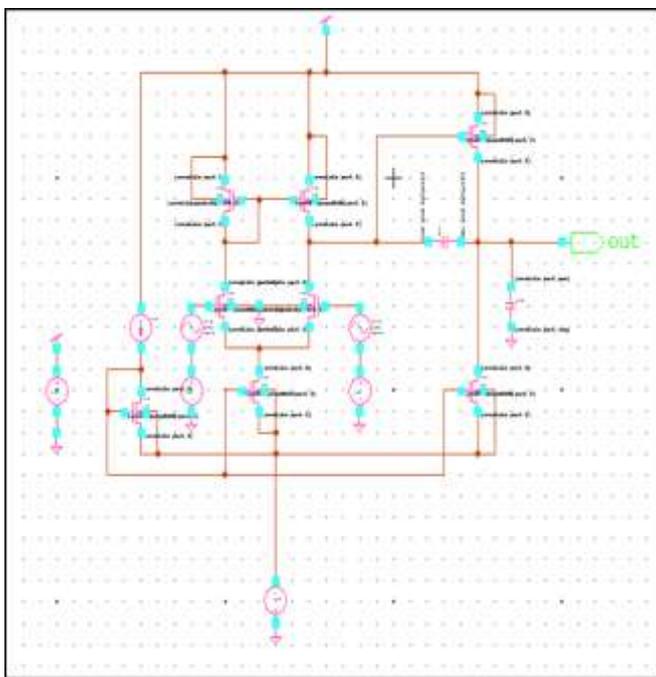| Specification Name	Value
Supply Voltage	2.5V
Bias Current	30µA
Compensation Capacitor	3pF
Load Capacitor	10pF
Offset Voltage	1.6V

Figure 4. Two Stage CMOS op-amp with SCMC

The MOS transistors aspect ratio variations affect the performance of the two stage CMOS op-amp. Therefore the aspect ratio has to be selected properly to optimise the performance of the circuit. The single capacitor miller compensation strategy has a drawback which is eliminated with the help of single capacitor in series with nulling resistor miller compensation strategy. This modified approach mainly either eliminates the RHP (right hand plane) zero or shift it to LHP(left hand plane). Figure 5 shows the schematic for the modified miller compensation technique for two stage CMOS op-amp for 180nm technology.
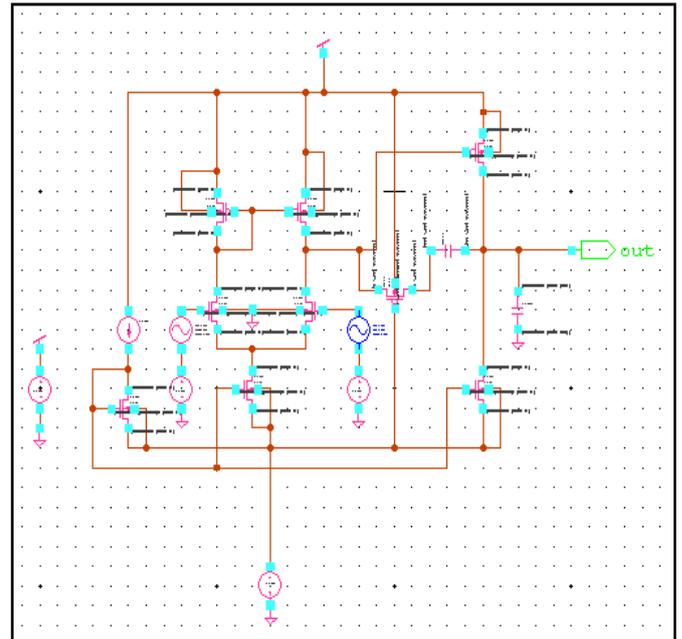

Figure 5. Two Stage CMOS op-amp Using SCMC with Nulling Resistor

IV.   SIMULATION RESULTS

A.   AC ANALYSIS
In Ac analysis, an ac signal is applied to both the terminals of the input stage. With the help of AC analysis we can estimate several performance parameters like gain, unity gain bandwidth, -3dB bandwidth, phase margin etc. The gain and phase margin is estimated using DC operating point and AC analysis.
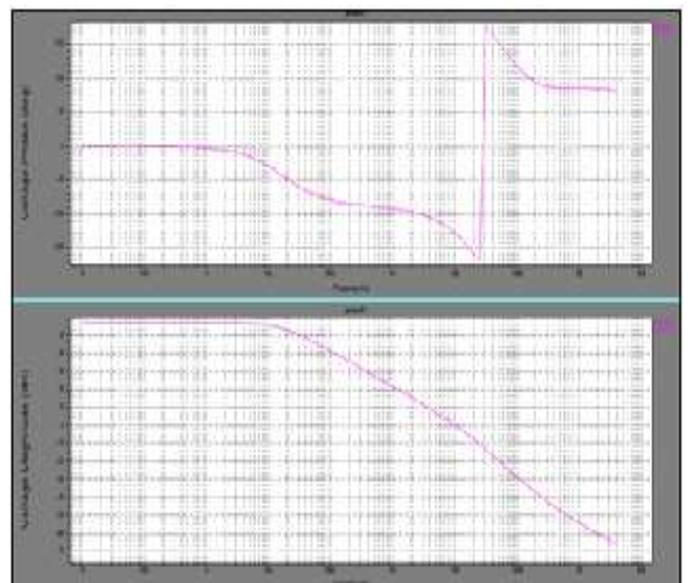

Figure 6. Frequency Response of Two Stage op-amp   with SCMC

TABLE 2. AC Analysis Output for Two Stage CMOS op-amp with SCMC

Parameter Name	Parameter Value
Gain	57.18dB
Unity Gain Bandwidth	10MHZ
3dB Bandwidth	115KHZ
Phase Margin	56 degree

Figure 7. Frequency Response of op-amp Using SCMC with Nulling Resistor

TABLE 3.AC Analysis Parameters for Two stage op-amp using SCMC with Nulling Resistor

Parameter Name	Parameter Value
Gain	48.27dB
Unity Gain Bandwidth	11.21MHZ
3dB Bandwidth	205KHZ
Margin	86.48egree

B. TRANSIENT ANALYSIS

*Slew Rate***:** A step from ground to voltage supply is applied to the non-inverting terminal of the input stage with the unity feedback configuration. The slew rate simulation is carried out performing a transient analysis using a pulse waveform. This step response is used for calculation of positive and negative

slew rate value for op-amp. Slew rate (SR) is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per second. The mathematical formula for slew rate is:

$$SR = \frac{\max\left(\ |dV_{out}(t)\ |\right)}{dt}$$

Where $dV_{OUT}(t)$ represents the output voltage of an amplifier as a function of time t. Figure 8 and figure 9 shows the step response for two different approaches of miller compensation technique for two stage op-amp.
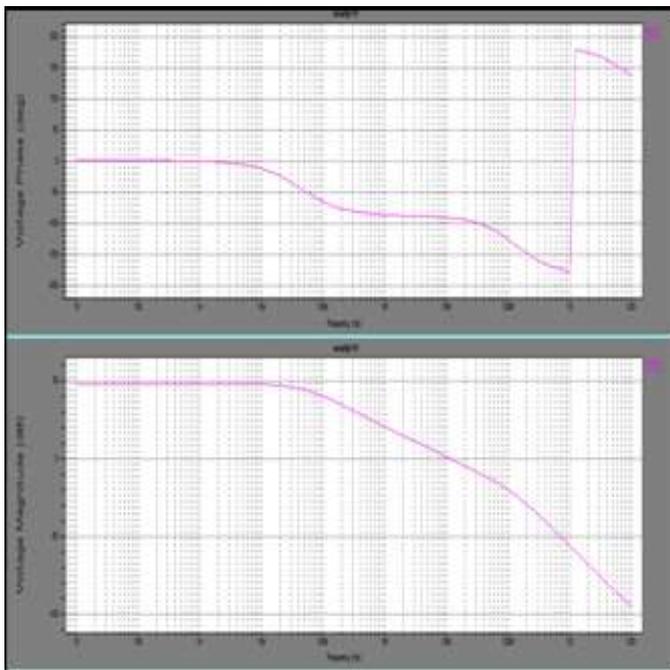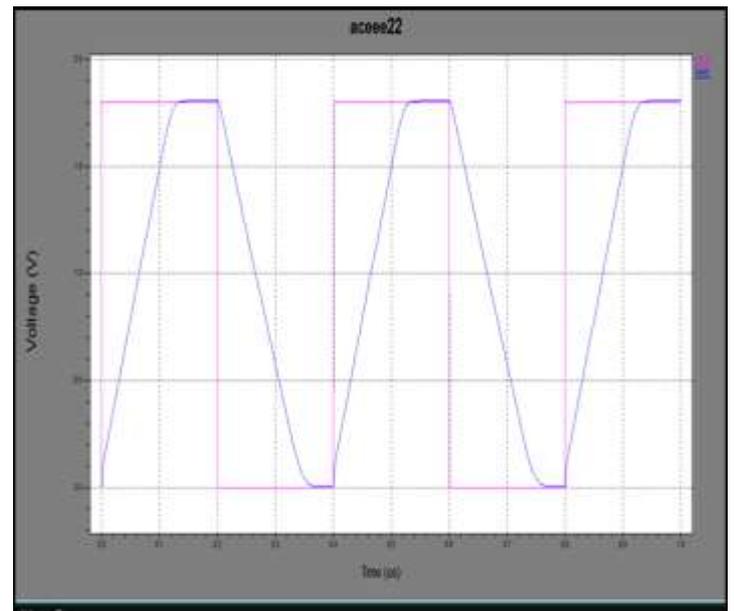

Figure 8. Slew Rate for Two Stage op-amp Using SCMC

The positive Slew Rate for two stage op-amp using single capacitor for miller compensation is 13.5 V/us and negative Slew Rate is 10.84 V/us.
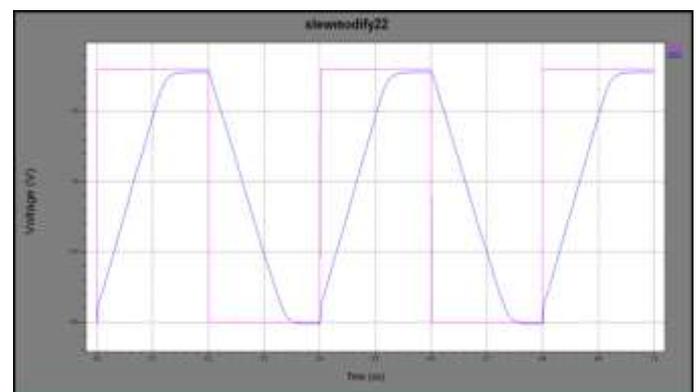

Figure 9. Slew Rate for op-amp Using SCMC with Nulling Resistor

The positive Slew Rate for two stage CMOS op-amp using miller capacitor in series with nulling resistor is 12.34 V/us and negative Slew Rate is 11.21 V/us.

Voltage Amplification: A transient simulation of the amplifier is an open loop gain configuration with the sinusoidal input at both the input terminal. The input applied to differential Amplifier is a 0.8mV and we are getting an output of 1.1 V. The simulated output for op-amp with SCMC is shown in Figure 10. Figure 11 shows the amplified output result for two stage CMOS op-amp using SCMC with nulling resistor.
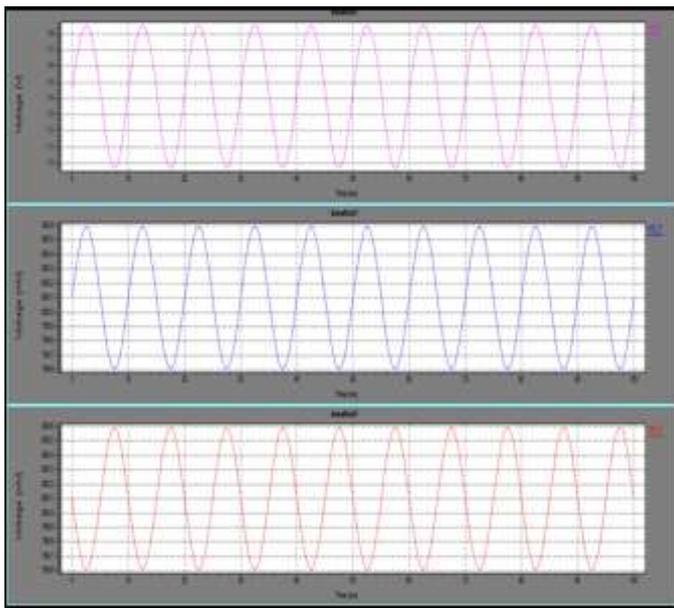

Figure 10: Output and Input Signals for Transient Analysis of op-amp with SCMC
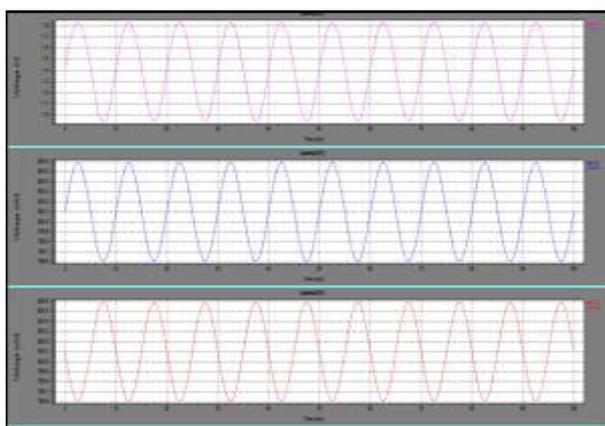

Figure 11: Input and output Response of Op-amp Using SCMC with nulling resistor

TABLE 4.Comparitive analysis of Performance Parameters for Miller Compenastion Approaches for 180nm Technology

Specification Parameters	Two Stage CMOS Op-amp with SCMC	Two Stage CMOS Op-amp with SCMC and nulling resistor
Gain(Av)	57.18 dB	48.27 dB
Unity Gain Bandwidth(UGB)	10MHZ	11.21MHZ
Phase Margin(PM)	56 degree	86.48 degree
3-DB Bandwidth	115KHZ	205KHZ
Positive Slew Rate	13.5 V/us	12.34 V/us
Negative Slew Rate	10.84 V/us	11.21 V/us
Load Capacitor(C_L)	10pF	10pF
Compensation Capacitor(Cc)	3 pF	3pF

IV.　　CONCLUSION

While designing several factors are taken into consideration such as area, power, supply voltage and current. Thus, to achieve optimized performance devices are scaled down accordingly.. Along with negative feedback configuration addition of each stage in multistage op-amps introduces another pole in the system which creates stability problem. For this reason, a miller compensation technique has been employed in system. In this paper two stage CMOS op-amp with miller compensation technique has been designed and simulated at 180nm technology. Two Stage CMOS op-amp with SCMC approach provides gain of 57.18dB and phase margin of 56 degree. In second approach, two Stage CMOS op-amp Using SCMC with Nulling Resistor increase the phase margin, which indirectly makes system more stable, miller compensation capacitor is used in series with nulling resistor, which provides gain of 48.27dB and phase margin of 86.48 degree. Apparently there is not a single point of scaling while designing, designers have to perform scaling depending upon the requirements or the specifications laid for a particular product.

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