FPGA Implementation of Area, Delay and Power Efficient Carry Select Adder Architecture Design

[1]Korra Ravi Kumar [2] Santhosh Kumar Allenki [3]G.Ramesh

[1]*ravikumar.korra@gmail.com*, [2]*santhosh.allenki@gmail.com*, [3]*ramesh.gajelli@gmail.com*

Abstract-The arithmetic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA are analyzed. CSLA have great scope by reducing area, power consumption delay. However the regular CSLA is still area consuming due to dual RCA structure, for reducing the area The CSLA can be implemented by using single ripple carry adder (RCA) and BEC converter. In this paper, we present an innovative CSLA architecture which replaces the BEC using D-latch. Substantiation of proposed design is done through design and implementation of 16-bit adder circuit. Simulated result shows that the proposed architecture achieves two advantages in terms of area and delay. Implementation is done in Artix7 FPGA kit. For simulation Xilinx ISE 14.7 is used.

Keywords—*CSLA , RCA , BEC , FPGA*

*****

I. INTRODUCTION

Design of low power, area-efficient and high speed data path logic systems are one of the most essential areas of research in VLSI. Adders also used in multipliers, in high speed integrated circuits, computers and Digital Signal processors (DSP).It is used to calculate adders, table indices and similar applications. In digital circuits speed of addition process is controlled by time required to propagate a carry through the adder. An adder plays important role in arithmetic unit. The sum of each bit position in initial adder is generated sequentially only after the previous bit position was added and a carry propagated into the next position. An efficient adder design essentially improves the performance of processor and integrated circuits. The major speed limitation of adders arises from the huge carry propagation delay occur in the conventional adder circuits such as ripple carry adder (RCA) and carry save adder (CSA). The advantage of carry select adder is its reduced propagation delay characteristic. It is implemented by using parallel stages that result from multiple pairs of ripple carry adder. The RCA generates initial sum and carry for the CSA structure by considering the carry input to be 0 and 1 respectively. The final sum and c_{out} output is chosen by the use of multiplexer[1] the c_{out} of the preceding block of the adder acts as the selected signal to the multiplexer, The multiplexers uses adders in their final stage and speed performance of multipliers is determined by the type of adders they actually employ[2][3] in addition process. He et al [4] proposed a square root (SQRT)-CSLA to implement large bit width adders with less deley. In a SQRT CSLA, CSLA with increasing size are connected in a cascading structure. The main objective of SQRT- CSLA design is to provide a parallel path delay. Ramkumar and kittur [5] suggested] a binary to binary to excess-1 converter (BEC) based CSLA. A CSLA based on common Boolean logic(CBL) is also presented in (6) and (7).The CBL based CSLA of [7] involves significantly less logic resource than the conventional CSLA but it has longer CPD which is almost equal to that of RCA. CSLA using basic unit block proposed in reference [8] of Sakthi kumaran and Bhaskaran, but area is increasing marginally.

This paper proposes an efficient method which replaces the RCA block using D-latch with enable. This paper aimed for the implementation of high performance optimized FPGA architecture. Xilinx ISE 14.7 used for simulation and synthesis. Implementation is done in ARTIX7 FPGA kit.

The rest of the paper organized as fallows section II presents a review of the conventional adder structures. Section III presents a BEC structure. Section IV presents the proposed CSLA architecture. Section V depicts the results of proposed adder circuit. Section IV concludes.

II. CONVENTIONAL ADDER CIRCUITS

Carry select adder constructed using the conventional 4-bit ripple carry adder. RCA uses multiple full adders to perform addition operation. Figure 1 shows the regular 16-bit carry select adder with two RCA blocks each for every 4-bit groups. The first 4-bit RCA block adds the 4-bits assuming c_{in} as 0. On the other hand, the second RCA adds the 4-bits with logic c_{in} as 1. The final sum is obtained based on the carry bit from the previous stage acts as the select signal for the multiplexer. Thus, the carry select adder achieves higher speed of operation at the cost of increased number of devices used in the circuit. This in turn increases the area and power consumed by the circuits of this type of structure.

ISSN: 2321-8169
2537 - 2540

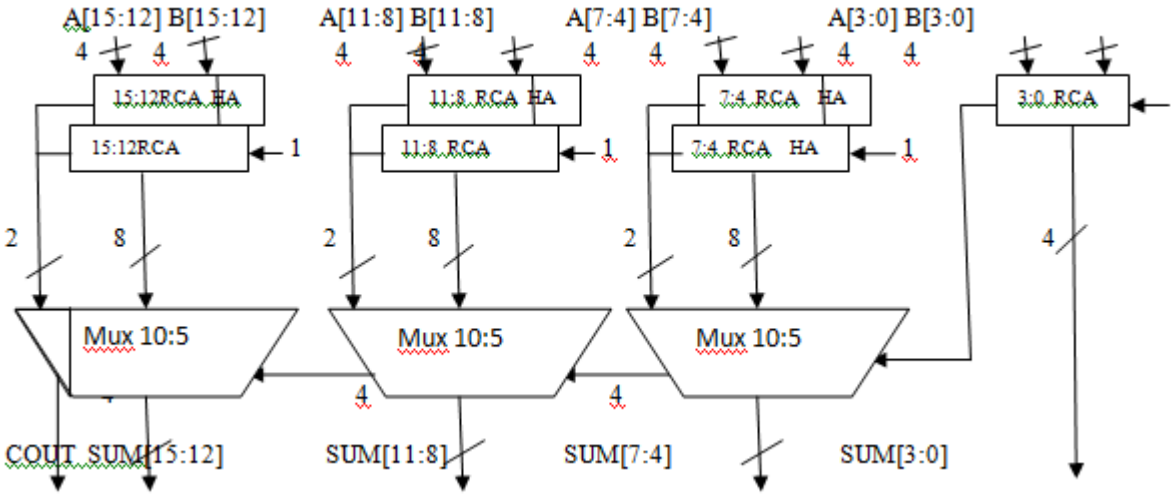

Figure 1.convensinal 16-bit Carry Select Adder

III. CSLA with BEC

Figure 2 shows binary to excess-1 converter (BEC) consists of 4 inputs and the result is obtained by addingn1 to input binary bit. Addition is achieved using BEC together with multiplexer. If select line of multiplexer is 0 then input (B3,B2,B1, and B0) is selected and assigned to the MUX output terminal else Binary to excess-1 converters output assigned to the MUX output terminal.

Equations of 4-bit BEC are given below.

$X_0 = !B_0$ .....

(1) $X1 = B_0 \wedge B_1$ .....

(2) $X_2 = B_2 \wedge (B_0 \& B_1)$.....

(3) $X_3 = B_3 \wedge (B_0 \& B_1 \& B_2)$..... .....(4)

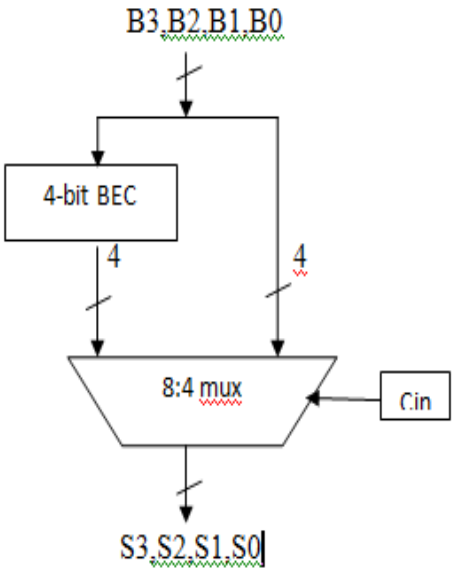

Fig. 2. 4-bit Binary to excess-1 converter with 8:4 multiplexer.

TABLE1: Truth table of4-bit binary to Excess-1 converter

Binary bits B3,B2,B1, B0,	Excess-1 X3, X2, X1, X0
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

IV. PROPOSED CSLA

The proposed method of carry select adder (CSA) replaces the second stage ripple carry adder (RCA) of conventional carry select adder by D-latch with enable signal. In sequential circuits latches are capable of storing single bit information output depend on enable signal, present and previous values.The outputs of latches

 ISSN: 2321-8169
2537 - 2540

continuously controlled by their inputs until the enable signal is active

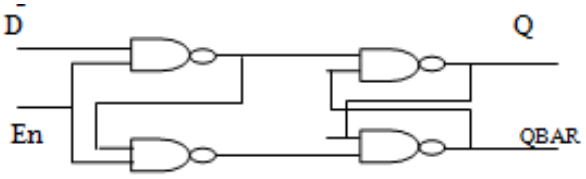

Fig.3.D-latch

In the proposed 16-bit modified carry select adder circuit organized into three stages the primary stage consists of four 4-bit ripple carry adder, second stage contains D-latches and stage three consists of multiplexers are there in which least significant bit (LSB) adder is ripple carry adder. The upper half of the adder that is most significant part is 12-bit wide which works based on the enable or signal. Note that the first(and only first) full adder may be replaced by a half adder. If the enable signal is active high addition operation for carry one is performed. Here latch is used to store the sum and carry for c_{in} =1. Carry output of previous stage LSB adder is used as a select signal

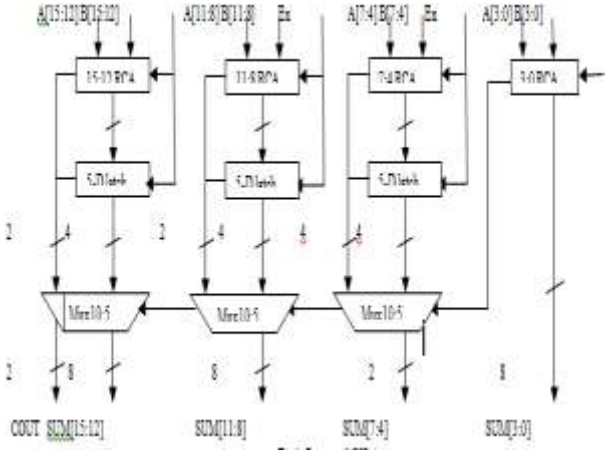

Fig.4. Proposed CSLA

Table II: Comparison of Adders for Delay, Area And power

Word size	Adder	Delay(ns)	Area(μm^2)	Power(mw)
16-bit	Carry select adder	0.95	1230.112	0.586
	BEC CSA	0.90	1015.121	0.512
	Proposed CSA	0.85	877.911	0.491

for multiplexer to select final carry and sum outputs. When c_{in} =1, then sum and carry of D-latch is selected or else MSB adder is accessed. The group 2 structure has five D-latches in which four are used to store sum4,sum5,sum6 and sum7 from second stage RCA and the last D-latch is used to store carry. Multiplexer is used as a selection device depending on incoming carry from previous stage. The 10:5 multiplexer are used in proposed architecture is the combination of 2:1 multiplexers. When the enable signal is at active low state a4,a5,a6,a7 added with b4,b5,b6,b7 here carry is equal to zero. When the enable signal is at active high state addition operation is performed with carry is equal to 1. All the latches are activated to store the sum and carry for carry is equal to one. Based on the value of c1 whether it is 0 or 1 the MUX selects the actual sum and carry, because of these latches gate count greatly reduced due to that area decrease, speed increases, delay decreases and power consumption decreases.

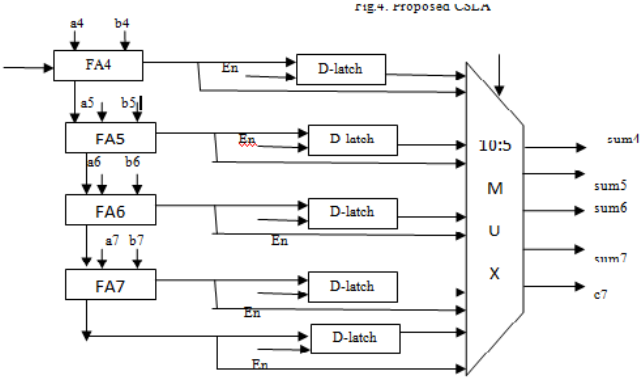

Fig. 5.: Group2 structureDelay and area count of blocks of CSLA

V. RESULTS

The carry select adder architecture design in this paper has been developed using Verilog-HDL and synthesized in Xilinx ISE 14.7 tool. Table2 Shows the post layout simulation results of both the conventional and proposed adder structure in terms of delay, area and power. The total power represents the sum of dynamic power, static power and leakage power.

VI. CONCLUSION

The conventional carry select adder (CSLA) uses two carry blocks, one block with carry is equal to 0 and the second one with carry input is equal to 1. The conventional CSA suffers from the disadvantage of occupying more chip area, which has been overcome by Binary to Excess-1 converter. The proposed carry select adder can be used to reduce the delay, area and power than the conventional and Binary to Excess-1 converter adder by using the D-latches,

VII. REFERANCES

[1] K.K.Pathi, VLSI digital signal processing. New York,NY,USA:wiley 1998
[2] A.P.Chandrakasan, N.Verma,&D.C.Daly,"Ultra low – power electronics for bio medical applications",Annu.Rev.Biomed.Eng.,Vol.10.PP.247-274.Aug.2008

[3] O. J. Bedrij, "Carry-select adder," IRE Trans. Electron. Comput., pp.340–344, 1962.
[4] Y.Kim&L.S.Kim,"64 Bit carry select adder with reduced area "Electron.lett.,Vol.37,No.10,PP.614-615,May 2001
[5] Y.He,C.H.Chang,&J.Gu."An area efficient 64 Bit square root carry select adder for low power application"in Proc.IEEE Int.Symp.Circuit syst.,2005,Vol.4,PP.4082-4085
[6] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, p. 53–58, 2010.
[7] L-C.Wey,C-C.Ho,Y-S.Lin&C.C.Peng," An area efficient carry select adder design by sharing the common boolean logic term",in proc.IMECS.2012,PP.1-4
[8] S.Manju&V.Sornagopal,"An efficient SQRT architecture of carry select adder design by common Boolean logic" in Proc.VLSI ICEVENT, 2013, PP.1-5

Korra Ravi Kumar received the Bachelor‟s Degree in the Department of Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, T.S. India in 2006 and Master‟s Degree in VLSI System Design from JNTU, Hyderabad, T. S. India in 2011. He is currently Associate Professor in the Department of ECE, Sree Chaitanya College of Engineering, Karimnagar, T.S. India, He has published three papers in International Conference and two papers in National Conference in the Testing area. His areas of interest include Low Power Very large scale integration (VLSI) Testing and Embedded System Design.

Santhosh kumar allenki received the Bachelor‟s Degree in the Department of Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, T.S. India in 2006 and Master‟s Degree in DSCE from JNTU, Hyderabad, T. S. India in 2011. He is currently Associate Professor in the Department of ECE, Sree Chaitanya College of Engineering, Karimnagar, T.S. India, He has published three papers in International Conference and two papers in National Conference in the Testing area. His areas of interest include Low Power Very large scale integration (VLSI) Testing and Embedded System Design.

Ramesh gajelli received the Bachelor‟s Degree in the Department of Electronics and Communication Engineering from Jawaharlal Nehru Technological University, Hyderabad, T.S. India in 2005 and Master‟s Degree in ES from JNTU, Hyderabad, T. S. India in 2011. He is currently Associate Professor in the Department of ECE, Sree Chaitanya College of Engineering, Karimnagar, T.S. India, He has published three papers in International Conference and two papers in National Conference in the Testing area. His areas of interest include Low Power Very large scale integration (VLSI) Testing and Embedded System Design.