Performance Analysis of FinFET Based Inverter circuit, NAND and NOR Gate at 22nm and 14nm Node technologies

Raju Hajare
Associate Professor
Dept. of Telecommuication Engineering
BMSIT
Bangalore, India

Sunil C
Dept. of Telecommunication Engineering
BMSIT
Bangalore, India
sunilc_93@yahoo.co.in

Anish Kumar A R
Dept. of Telecommunication Engineering
BMSIT
Bangalore, India
10anishkumar.ar@gmail.com

Sumanth Jain P R
Dept. of Telecommunication Engineering
BMSIT
Bangalore, India
sumanth143jainpr@gmail.com

Sriram AS
Dept. of Telecommunication Engineering
BMSIT
Bangalore, India
sriram191994@gmail.com

Abstract— The size of integrated devices such as PC, mobiles etc are reducing day by day with multiple operations, all of these is happening because of the scaling down the size of MOSFETs which is the main component in memory, processors and so on. As we scale down the MOSFETs to the nanometer regime the short channel effects arises which degrades the system performance and reliability. Here in this paper we describe the alternative MOSFET called FinFET which reduces the short channel effects and its performance analysis of digital applications such as inverter circuit, nand and nor gates at 22nm and 14nm node technologies.
Keywords- *FinFET, PTM, Technology node, Power, delay*

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I. INTRODUCTION

There have been many significant advances in nanoelectronic materials and devices during the first decade of the 21st century, but nowhere it has the impact of shrinking devices to the nanoscale been more dramatic than in the semiconductor industry. For over 30 years, the industry has been able to double the number of field-effect transistors on a chip every 18-24 months, a trend that has come to be known as "Moore's Law". The speed of the FET went up while the area occupied by the device and power used by the device went down, so that the power density remained constant.

Virtually Integrated Circuits rule the world. Laptops, I-pads and other digital appliances are now indissoluble parts of the structure of modern life. [1] CMOS is a technology for constructing integrated circuits. High noise immunity and low static power consumption are the two key factors of CMOS. Considerable power is only used during the switching process of the transistors in the CMOS devices. Also CMOS devices do not produce thermal noise as other forms of logic, for example Transistor-Transistor Logic (TTL). It allows a high density of logic functions on a chip. This made the CMOS an adorable technique for the use in IC Technique.

The past 3 decades CMOS IC technologies have been scaled down continuously and entered into the nanometer region for various applications. [2] In many designs the need of memory has increased vastly from consumer goods to industrial applications. It increases the necessity of improving memories in a single chip with the help of nanometer technologies. There are lots of applications and integrated memories are improved using nanotechnology and every circuit consists of an inverter or nand or a nor circuits too.

The shrinking of the CMOS technology has been increased very aggressively with ultra-thin sizes. [3] This shrinking of the design creates many significant challenges and reliability issues in design which causes augmented process variations, short channel effects, power densities and leakage currents etc.

Every device consists of circuits comprising of an Inverter, nand or nor gates. Thus we can say it is one of the essential part of any circuit for a device. The operations of such device is usually valued by taking its operation parameters like switching speed in terms of delay of operation, power consumption and power dissipation. Since the MOSFET's failure at the nanometer regime beyond 32nm and our focus is on operations at the lower node technology such as 22nm and 14nm where alternative MOSFET called FinFET comes into picture and its performance must be studied and prove it is the solution for conventional MOSFET's failure.

The paper is organized as follows: section II gives a short description about the MOSFET and FinFET and their structure's description, section III gives the details about the software used, the PTM models and the design considerations, section IV describes FinFET based digital applications such as the designed FinFET inverter circuit, the FinFET nand gate circuit, FinFET nor circuit and and their simulation results obtained. section V focuses on the discussion on all the results

obtained and finally section VI provides conclusion on the current work done.

II. FIN BASED FIELD EFFECT TRANSISTOR TECHNOLOGY,

The metal–oxide–semiconductor field-effect transistor (MOSFET) is a transistor used for amplifying or switching electronic signals. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, the body (or substrate) of the MOSFET is often connected to the source terminal, making it a three-terminal device like other field-effect transistors. Because these two terminals are normally connected to each other (short-circuited) internally, only three terminals appear in electrical diagrams. The MOSFET is by far the most common transistor in both digital and analog circuits.

The 'metal' in the name MOSFET is now often a misnomer because the previously metal gate material is now often a layer of poly silicon (polycrystalline silicon). Likewise, the 'oxide' in the name can be a misnomer, as different dielectric materials are used with the aim of obtaining strong channels with smaller applied voltages. Figure 1 shows the structure of MOSFET, the body terminal is not shown for the sake of simplicity.

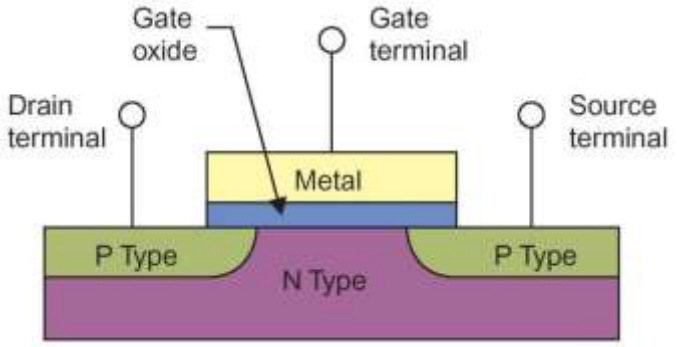

Fig. 1: MOSFET structure

The scaling of the commercially popular bulk MOSFETs becomes increasingly difficult for gate lengths below ~20nm (sub-45 nm half-pitch technology node). As the gate length is reduced, the capacitive coupling of the channel potential to the source and drain increases relative to the gate, leading to significantly degraded short channel effects (SCE), namely [4]: Channel length modulation, Drain induced barrier lowering (DIBL), Velocity saturation, Oxide Breakdown.

To deliver small and fast IC's with large computation capability, key requirements of transistor design are:

1. High ON current (ION).
2. Low OFF current (IOFF)
3. High switching speed.

To achieve these, other transistor options which will give the better performance, must be explored. That is the place where FinFET technology plays a pivotal role.

The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by thin silicon "fin", which forms the body of the device [5]. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device. The wrap-around gate structure provides a better electrical control over the channel and thus helps in reducing the leakage current and overcoming other short channel effects. Figure 2 shows the structure of FinFET. In the technical literature, FinFET is used somewhat generically to describe any fin-based, multi-gate transistor architecture regardless of number of gates. FinFET can also have two electrically independent gates, which gives circuit designers more flexibility to design with efficient, low-power gates.

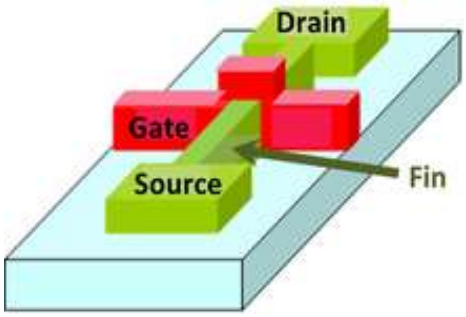

Fig. 2: FinFET structure

The primary obstacles to thescaling of CMOS gate lengths to 22nm and beyond includes short channel effects, sub-threshold leakage, gate-dielectric leakage and device to device variation reduction which leads low yield. The International Technology Roadmap for

Semiconductors (ITRS) predicts that double gate or multi-gate devices will be the perfect solution to obtain the device with reduced leakage problems and less channel length of the transistor. The FINFET based designs are known as double gate device which offers the better control over short channel effects, low leakage current and better yield in 22nm and beyond which helps to overcome the obstacles in scaling [6].
When threshold voltage Vt is less than a potential voltage, gates of the double gate or FINFET device activates the currently flow between drain to source with modulating the channel from both the sides instead of one side. The potential which is applied to two gates together influence potential of the channel which fighting against the drain impact and leads to solve and give the better shut off to the channel current and reduces Drain Induced Barrier Lowering (DIBL) with improved swing of the design. This FINFET based transistors offers good trade off for power, area as well offering interesting delay.

III. SOFTWARE, MODEL AND DESIGN CONSIDERATIONS

A. Hspice simulation software

The circuit simulations are done using Hspice by synopsys. HSPICE is an optimizing analog circuit simulator. Which we have used it to simulate electrical circuits in transient domain. HSPICE is best suited for fast, accurate circuit and behavioral simulation. It facilitates circuit-level analysis of performance

Simulations at the integrated circuit level and at the system level need proper planning of the organization and interaction between transistor models and sub-circuitry. Methods that work for small circuits could have too many limitations for some other higher-level simulations.

Numerical simulations based on finite element methods, or TCAD tools, are useful for technology evaluation and design exploration of FinFET-based circuits. [7] Mixed-mode TCAD simulations can be combined with Monte Carlo to predict the impact of device variation on circuit performance. However, a large number of simulations is needed and such task is time consuming. An efficient compact model (or SPICE model) like BSIM-CMG is more suitable. The model employs physical expressions to capture the effect of device parameters such as L and Tfin on the electrical characteristics of multigate devices.

Through proper parameter extraction, the effects of these variation sources can be captured. Hence Hspice is efficient tool for the current scenario of our operations.

B. Technology nodes

Technology node is referred to as the half pitch distance between two transistors, it can also be defined as the smallest gate length allowed for a device to operate without having adverse effects hinder its performance. Gate length is not exactly the same as the technology node. Different fabricators have different requirements from their clients and may change the deice gate length to suit their needs. However, in most cases it ends being the same. The 22-nanometer (22-nm) is the process step currently being used. The typical half-pitch (i.e., half the distance between identical features in an array) for a memory cell using the process is around 22 nm. The 14-nanometer (14 nm) node is the technology node following the 22-nm/ (20 nm) node. All foundries already started designing the IC's using 14-nm node. But it has been said that every attempt to miniaturize the size of the device will results in lot of difficulties. Same applies to 14-nm node; hence designing IC's using this node also has some challenges, which needs to be faced carefully.

Fig. 3: Roadmap of the node technology

Fig. 3 shows the node technology roadmap where we can see that 22nm node is currently in the process of usage and in the future 14nm and beyond will be the available device's node technology.

C. Predective technology model

The Predictive Technology Model (PTM) or PTM provides accurate, customizable, and predictive model files for future transistor and interconnect technologies. These predictive model files are compatible with standard circuit simulators, such as SPICE, and scalable with a wide range of process variations. With PTM, competitive circuit design and research can start even before the advanced semiconductor technology is fully developed. In our work we are using the 22nm and 14nm PTM multi gate models for the FinFET circuit simulations using Hspice.

D. Design considerations

The design considerations is one of the important step in developing a spice model and then simulating it. The design parameters are considered with respect to the PTM model files. Table 1 shows the design parameters we have employed for the circuit simulations in our present work.

PARAMETER	14nm FinFET	22nm FinFET
Gate Length (Lg)	14nm	22nm
Supply Voltage	0.8v	0.9v
Thickness of Fin (tfin)	10nm	10nm
Height of Fin (Hfin)	23nm	30nm
Thickness of oxide (tox)	1.3nm	1.4nm

Table. 1: Design considerations

The above shown design parameters are important in designing any circuit using FinFET. Node technologies are defined based on the gate length, as the device is scaled down the supply voltage fin, oxide thickness and height of the fin is also is scaled down too meet the requirements and to avoid the velocity saturation factor. The design considerations are done on the basis of the geometry description of FinFET device structure. Fig. 4 shows the geometry description of FinFET.

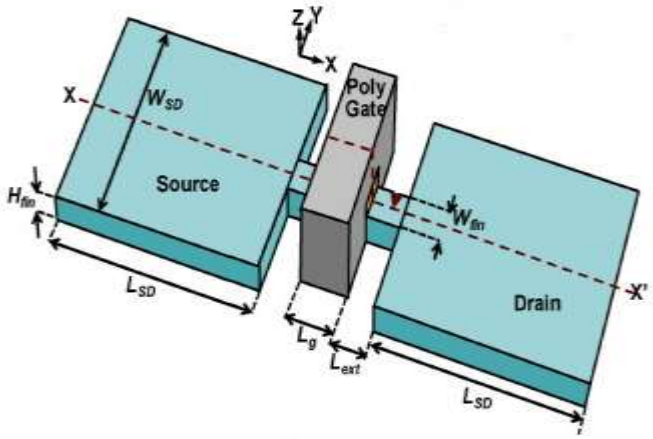

Fig. 4: Geometry description of FinFET

The important parameter and equations through which the design considerations are made are:

Where,
Hfin: Height of the fin.
Wfin: Width of the fin.
LSD: Length of the source and drain.
WSD: Width of the source and drain.
Lg: Length of the Gate.
Lext: Length of the source and drain extension.
Effective width (Weff) of the device is given by,

$$Weff = 2Hfin + Wfin$$

And effective length of the channel is given by,

$$Leff = Lg - 2\delta Lg$$

Where, δLg is the gate underlap length.

 ISSN: 2321-8169
2527 - 2532

IV. FINFET BASED DIGITAL APPLICATIONS

A. *FinFET based Inverter*

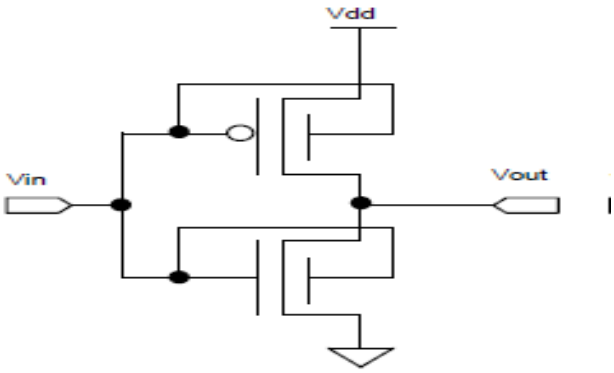

Fig. 5: FinFET based inverter

Fig. 5 shows the FinFET based where inverter, it is visible from the circuit that the FinFET consists of gates on the either side of the channel. We are considering the short gated (SG) model for our study and circuit design but we can also develop the circuit with independent gate (IG) model which possibly provides better control over the channel. The working of the circuit is similar to that of a basic cmos or mosfet inverter.

By using the Hspice and PTM model file the spice model for FinFET inverter circuit is developed and simulated and the parameters delay, average power consumption, maximum power consumption and power dissipation are calculated.

PARAMETER	14nm FinFET Inverter	22nm FinFET Inverter
Delay	74.0142 ps	45.4625 ps
Avg Power	3.2797 uW	4.5646 uW
Max Power	28.0496 uW	65.5722 uW
Power dissipation	393.9912 fW	414.8270 fW

Table. 2: Simulation results for FinFET inverter
ps-pico seconds, uW- micro watts, fW- femto watts

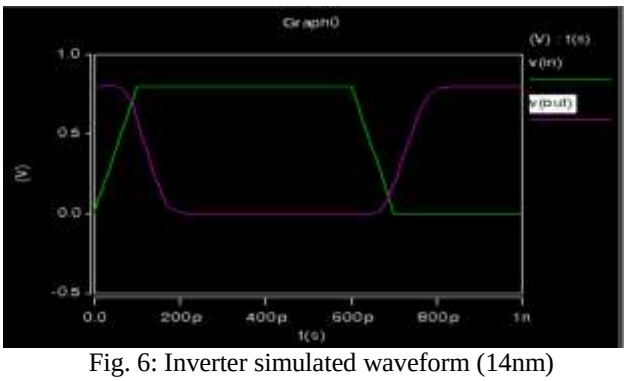

Fig. 6: Inverter simulated waveform (14nm)

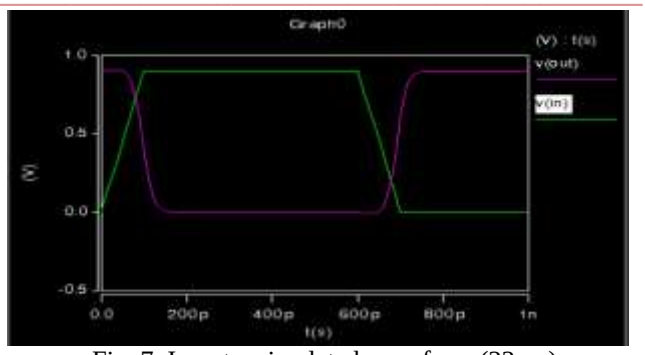

Fig. 7: Inverter simulated waveform (22nm)

Fig. 6 and 7 shows the simulated waveform of FinFET based inverter at 14nm and 22nm respectively. The green colored wave indicates the input and the pink indicated the output waveform. The slight variations in each graph is because of the scaling of FinFET.

B. *FinFET based NAND gate*

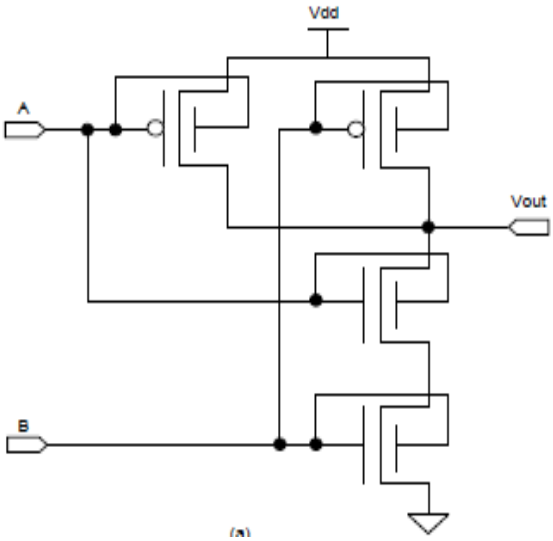

Fig. 8: FinFET based NAND gate circuit

Fig. 8 shows the FinFET based nand gate circuit. The results obtained on the simulation of the above circuit is tabulated in table. 3 as follows:

PARAMETER	14nm FinFET NAND	22nm FinFET NAND
Delay	72.2176 ps	42.4052 ps
Avg Power	85.2171 nW	119.2689 nW
Max Power	35.2913 uW	117.8822 uW
Power Dissipation	161.5540 fW	614.8488 fW

Table. 3: Simulation results for FinFET based NAND gate

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2527 - 2532

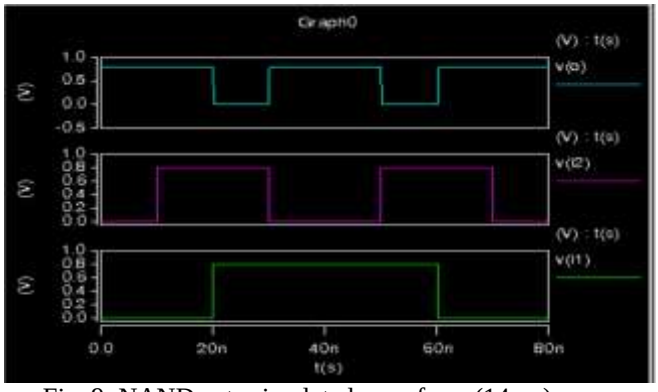

Fig. 9: NAND gate simulated waveform (14nm)

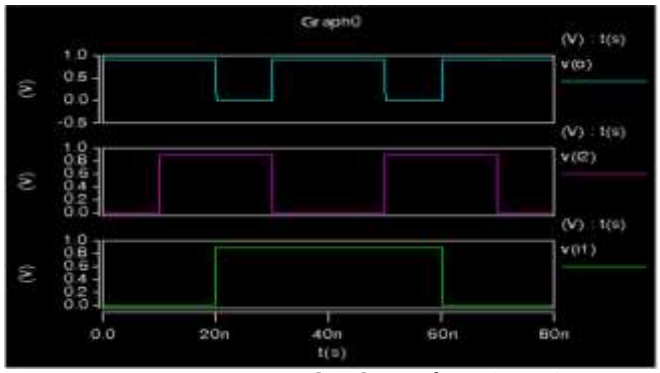

Fig. 10: NAND gate simulated waveform (22nm)

Fig. 9 and 10 shows the simulated waveform of FinFET based NAND gate at 14nm and 22nm respectively. The green colored waveform indicates input 1, pink indicates input 2 and blue indicates the output. It is quite clear from the above figures that the variations indicates the scaling of the gate lengths of the device and the results obtained and tabulated in the above table is evident and clearly distinguishes the result and support the output results of waveforms.

C. FinFET based NOR gate

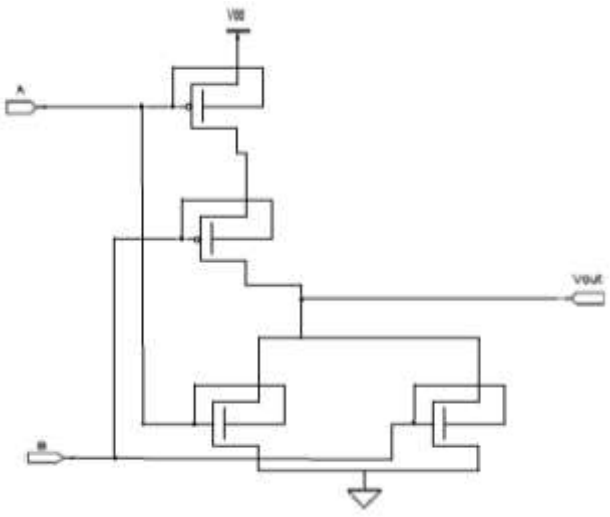
Fig. 11: FinFET based NOR gate circuit

Fig. 11 shows the FinFET based NOR gate circuit. The simulation results obtained using the Hspice is tabulated in table. 4

PARAMETER	14nm FinFET NOR	22nm FinFET NOR
Delay	86.2274 ps	51.0154 ps
Avg Power	87.2265 nW	123.9511 nW
Max Power	32.311 uW	67.1310 uW
Power Dissipation	788.2441 fW	829.5558 fW

Table. 4: Simulation results for FinFET based NOR gate

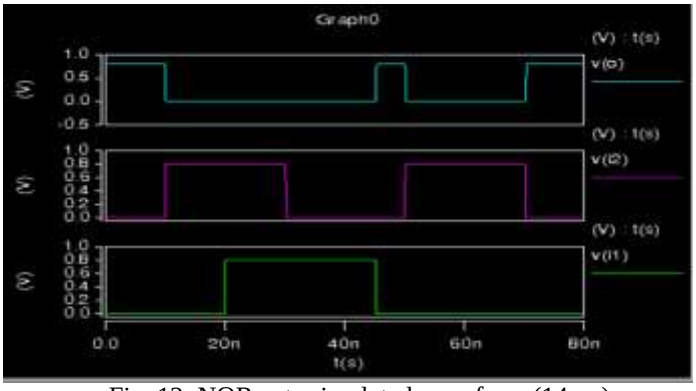

Fig. 12: NOR gate simulated waveform (14nm)

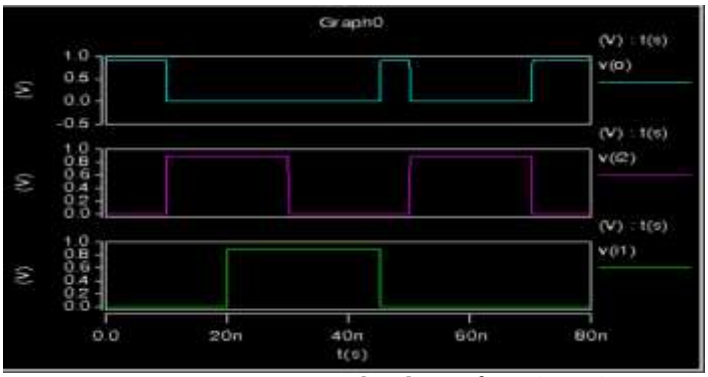

Fig. 13: NOR gate simulated waveform (22nm)

The simulated waveforms variations are perfectly supported by the results obtained. The colour indications are same as that of the NAND gate waveforms.

V. RESULTS AND DISCUSSION

The results obtained for each of the digital application at 14nm and 22nm of FinFET shows a system tradeoff. The system tradeoff is a concept in which a system trade any of the parameter such as delay, power and area in order to obtain better results. Hence to obtain something the system need trade something else. In the above results it is clear that the tradeoff is happening between delay with power and area.

As we scale down the device from 22nm to 14nm the area covered by the device is reduced, the power consumption hence the power dissipation is also reduced but the delay in the operation of the device has increased at the 14nm node. This is very minor issue because the system reliability and the

performance has improved because of this tradeoff and the tolerant capacity of the device is also improved.

VI. CONCLUSION

Simulation results for FinFET based digital application at nanometer regime of 22nm and 14nm are studied here. The results obtained shows that the FinFET's application on the nanoscale devices has improved giving better results than the traditional MOSFETs. The short channel effects which were faced by the MOSFET devices hence failing to operate at lower technology nodes has overcome by the FinFET. Hence FinFET is a promising candidate in the current and future IC fabrication process and the modern devices can possess FinFET based circuits and perform better with more features, with more speed and low power consumption and dissipation.

VII. FUTURE SCOPE

The FinFET based applications can be extended to various field such nano robots, biosensing etc. The device performance may be also improved by using alternate materials like carbon nano tubes or graphene. This could increase the speed of operation and provides better control over the channel and reduces power consumption.

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