FPGA Based Notch Filter to Remove PLI Noise from ECG

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***Abstract*—**in the context of heart disease ecg found to be major contributor for diagnosis purpose, always the recorded ECG signal is corrupted by different types of noise and interference due to surrounding environmental situation. Powerline noise is one of the prominent noises that corrupt and masks valuable information of ECG signal and mainly occurs when electrodes are poorly attached to the body surface or when an external source such as the sinusoidal 50Hz signal interferes with the ECG signal. Hence it is necessary to remove this powerline noise with appropriate signal processing and here it is accomplished by implementing digital FIR filter using distributed arithmetic architecture based on FPGA using Xilinx system generator with MATLAB. By comparing different types of FIR notch filter with output SNR, adders, and multipliers required for removal of power line interference, it can be analyzed that equiripple method takes more elements for computation eventually computation time is high so it is difficult to apply equiripple type digital filter on noisy ECG signal. But the Output SNR is more for equiripple and least square design. It is observed that, FPGA is more efficient than DSP as it requires less power. Also better results have been observed for FPGA as compared to DSP for real time application.

Keywords*-ECG; FIR; MATLAB; Simulink; FPGA; Distributed Arithmetic.*

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I. INTRODUCTION *(HEADING 1)*

The electrocardiogram (ECG) depicts the electrical activity of the heart. ECG processing is a topic of great interest within the scientific community because of two reasons: (1) ECG is collected by non invasive means, which allows easy and wide availability and (2) the ECG contains very much information, which is highly valuable for diagnosing. The electrocardiogram is a surface measurement of the electrical potential generated by electrical activity in cardiac tissue. The ECG is a non-invasive diagnostic tool which was first put to clinical use in 1903 with Einthoven's invention of the string galvanometer. Einthoven's recording is known as the "three lead" ECG, with measurements taken from three points on the body. The difference between potential readings from right arm (RA) and left arm (LA) is used to produce the output ECG trace. The right leg (RL) connection establishes a common ground for the body and the recording device. For this work, this configuration is selected due to its simplicity and scalability. These heart potentials, detected with surface electrodes and generated with each heart beat, are characterized by a PQRST complex wave. Fig.1 shows typical ECG signal.

The ECG signal amplitude acquired from the electrodes is in the 0.1–5mV range with heart rates (R–R intervals) in the 0.5–3.5 Hz range. When this signal is acquired, it is always mixed with artifacts, which in electrocardiography refer to something that is not produced by heart beats themselves. These artifacts include, but are not limited to, electrical interference by external sources, electrical noise from elsewhere in the body, poor contact, and machine malfunction. Artifacts are extremely common, and knowledge of them is necessary to prevent misinterpretation of the heart rhythm. The most typical artifact is the power line interference, i.e., the electromagnetic radiation collected by the human body from the power lines, which include the 50/60 Hz component and its harmonics. The muscle tremor (electromyography) produces an artifact that is an electric noise added to ECG signal. The patient movement adds this artifact as a baseline wandering of the ECG signal. From various artifacts the Power line interference is easily recognizable since the interfering voltage in the ECG may have frequency 50 Hz. Hence, biomedical signal processing has become an indispensable tool for extracting clinically significant information hidden in the signal. Processing methods not only mimic manual measurement and support the diagnosis made by a physician but also extract features or information that cannot be obtained by mere visual assessment but provides valuable clinical information.

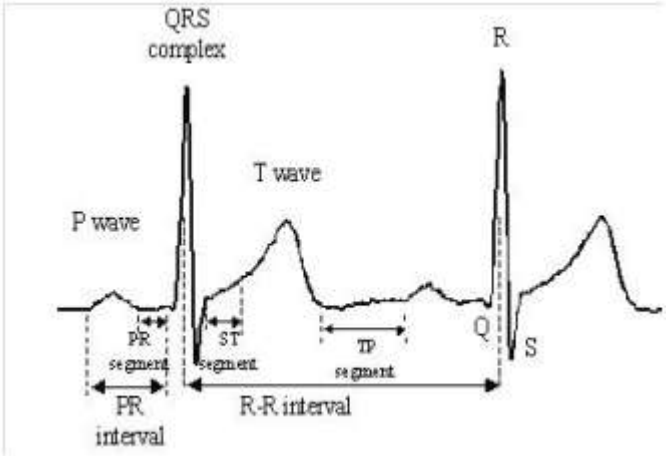

Fig. 1: Typical ECG Signal

Digital filters plays very significant role in the analysis of the low frequency components in ECG signal. Finite Impulse Response (FIR) filters are the most basic digital signal processing system components. It is at any rate the frequency with a strictly linear phase frequency. There is no input to output feedback, which is a stable system. Distributed algorithms preferred over traditional algorithm because they can greatly reduce hardware size utilization which results into high speed of execution. Recently, as is widely used in recent

FPGA digital signal processing, distributed algorithm in the FPGA to achieve the FIR digital filter to become very real needs.

II. FIR FILTER THEORY

The basic structure of FIR filter is like a sub-section of the delay lines. Each section of the output of the weighted cumulative, you can get the output of filter. Mathematical expression is:

$$y(n) = \sum_{k=0}^{L-1} h(k)x(n-k) \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

The corresponding pulse sequence is a unit of output *h(k)* and input *x(n)* of the convolution. Through the convolution relationship diagram can be directly drawn structure. It is called direct-type structure, as shown in Figure 2. In equation (1), *y (n)* is the n-time filter output, L is the number of FIR filter taps, *h(k)* is the k-class tap coefficient (unit impulse response), *x (n - k)* for k-tap delay the input signal. Figure 2 shows the N-order direct form FIR filter structure. It is committed by a "tapped delay line" adder and multiplier set constitutes. Each *y (n)* the output should be carried out *N* times multiplications and *N - 1* times to calculate the product and the addition.

FIR digital filter transfer functions as follows:

$$H(z) = \sum_{k=0}^{N-1} h(k)z^{-k} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

In which, h (k) is the filter coefficients as shown in fig.2. By the use of MATLAB can be easily derived FIR filter coefficients.

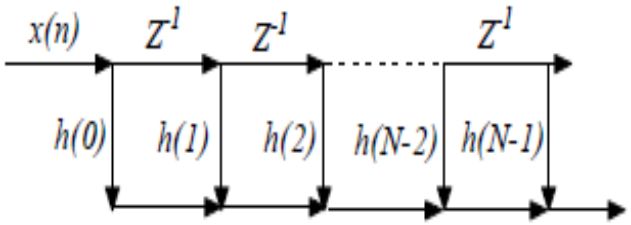

Fig.2: Convolution FIR filter structure

III. THE THEORY OF DISTRIBUTED FIR FILTER

Distributed arithmetic was first proposed by Crosier in 1973. But until Xilinx invented FPGA lookup table's structure, distributed arithmetic was widely applied in the calculation of the product.

Filter equation is rewritten as follows:

$$y(n) = \sum_{k=0}^{L-1} h_k x_k(n) \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Input data $x_k(n)$ can be used to represent B+1 bit complement that is:

$$x_k(n) - 2^B X_{k,B}(n) + \sum_{b=0}^{B-1} X_{k,b}(n)2^b, x_{k,b}(n) \in [0,1]$$

$$\ldots\ldots\ldots\ldots\ldots (4)$$

In equation (4), B for data bits wide, $x_{k,b}(n)$ on behalf of $x_k(n)$ the b-bit, $x_{k,B}(n)$ is the sign bit. Be (3) into (2) were:

$$y(n) = \sum_{k=0}^{L-1} h_k[-2^B x_{k.B}(n) + \sum_{b=0}^{B-1} x_{k,b}(n)2^b] - 2^B \sum_{k=0}^{L-1} h_k x_{k,B}(n) + \sum_{b=0}^{B-1} 2^b[\sum_{k=0}^{L-1} h_k\ x_{k,b}(n)]$$

$$\ldots\ldots\ldots\ldots\ldots (5)$$

By the equation (5) can be seen that entry in square brackets mean that all delayed the first b-bit input data and filter coefficients of each tap h_0, $h_1, h_2 \ldots\ldots h_{L-1}$, for the corresponding multiplication operator, and summation. Therefore, you can build a look-up table through the internal FPGA. In advance of all possible "and value" stored in the table. The actual calculation of the process of using all the input data into the corresponding bit combination of the vector as the address of the look-up table to address, it can direct access to this and value. The index part of sum results of the corresponding bit of the right, through the shift to achieve, logic resource utilization [3].

IV. FIR FILTER IMPLEMENTATION USING DISTRIBUTED ARITHMETIC ALGORITHM (DA)

Basics of Distributed Arithmetic (DA) are all additions and multiplications are replaced by shift-accumulator and Look up Table. DA design has a important prerequisite [1], [2] i.e., filter coefficients are known and simply c[n]x[n] gets multiplied with constant. This methodology is powerful because it reduces size of parallel multiply-hardware which is well suited to FPGA designs.

The block diagram of FIR filter using DA is shown in Figure 3. When DA is used it is necessary to store the inputs equal to the coefficient length after taking inputs all coefficients are taken to LUT i.e., 2n word. LUTs are preprogrammed for accepting n-bit address [2]. While computing individual mappings are done by weighting by the appropriate power of two factors. By using shift-adder it is efficiently implemented as shown in figure 4. While implementing on hardware shift a accumulator content by 1 bit to right instead of shifting each value by power factor using a shift adder, which requires an expensive barrel shifter.

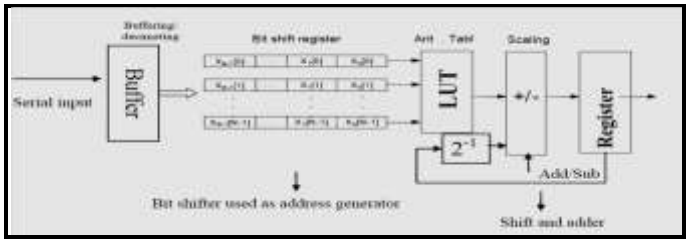

Fig. 3: Block diagram of DA implementation of a FIR filter [2].

V. IMPLEMENTATION

Figure: 4 & 5 shows, Simulink model for Distributed arithmetic based FIR filter design using DA_FIR v9.0 and Simulink

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model for Distributed arithmetic based FIR filter design using FIR Complier 5.0 respectively**.** Table 1 shows the comparison of different types of FIR notch filter with output SNR, adders, multipliers required for removal of power line interference at the same time fig. 6 shows Snap shot of ISE report generated from System Generator which added here for authenticate implementation. As compare to windowing method, equiripple method takes more elements for computation eventually computation time is high so it is difficult to apply equiripple type digital filter on noisy ECG signal. But the Output SNR is more for equiripple and least square design. So, for implementation these two designs are chosen also, Output waveforms for Equiripple and least square design is shown as observed in wave scope.

Table 1- Comparison of Different FIR notch filter Design

Type of FIR Filter	Filter order	SNR at Output	Multipliers	Adder
Equiripple	582	6.5813	583	582
Least Square	298	6.2989	299	298
Bartlett	298	5.6807	297	296
Blackman	298	5.6807	299	298
Hamming	298	5.8247	299	298
Hann	298	5.1973	297	296
Rectangular	298	6.2724	299	298
Kaiser	298	6.2036	299	298

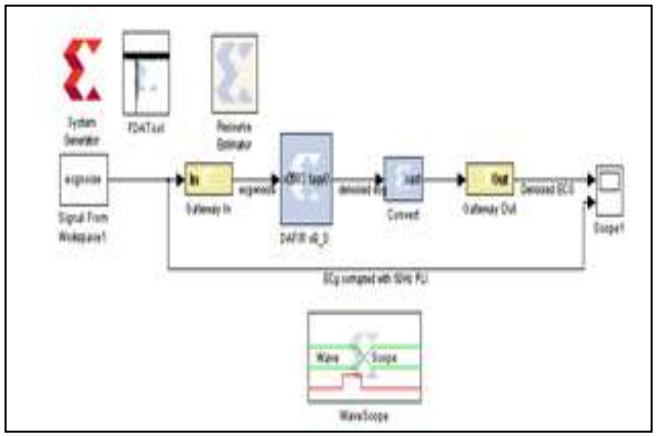

Fig.4: Simulink model for Distributed arithmetic based FIR filter design using DA_FIR v9.0

The HDL code for designed FIR notch filter is generated using ‘generathdl’ command in MATLAB. Another way to implement the design on FPGA is use Simulink tool of MATLAB [6]. For designing Simulink model compatible to FPGA device Xilinx blocksets are used. So replace Simulink blocks by Xilinx block.

Simulink model using Xilinx blocksets like DA FIR v9.0 or FIR Compiler 5.0 is as shown in figure 4 and 5. Result after implementation on Spartan 3E device is shown in figure 6.

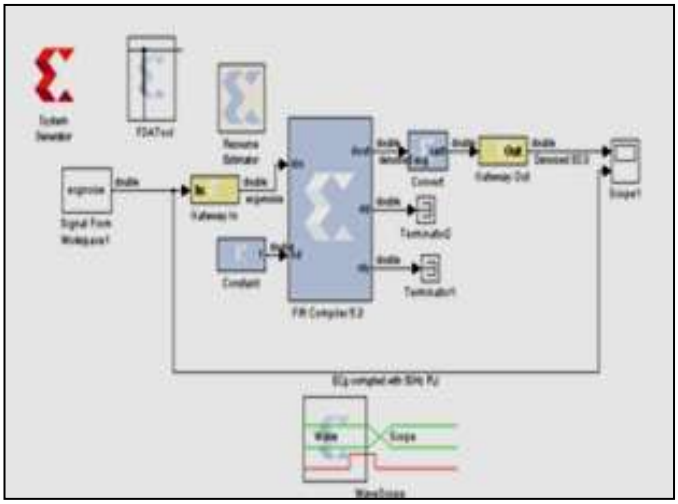

Fig. 5: Simulink model for Distributed arithmetic based FIR filter design using FIR Complier 5.0

Configuration File:	da_filter_cw.xreport	Parser Errors:	No Errors
Module Name:	da_filter_cw	Implementation State:	Mapped
Target Device:		• Errors:	No Errors
Product Version:	ISE 12.3	• Warnings:	125 Warnings (125 new)
Design Goal:	data unavailable	• Routing Results:	
Design Strategy:	data unavailable	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	2,201	9,312	24%	
Number of 4 input LUTs	2,035	9,312	21%	
Number of occupied Slices	1,387	4,656	29%	
Number of Slices containing only related logic	1,387	1,387	100%	
Number of Slices containing unrelated logic	0	1,387	0%	
Total Number of 4 input LUTs	2,060	9,312	22%	
Number used as logic	1,416			
Number used as a route-thru	25			
Number used as Shift registers	619			
Number of bonded IOBs	18	190	9%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.63			

Fig 6: Snap shot of ISE report generated from System Generator

Fig. 7: Output waveforms for Equiripple design

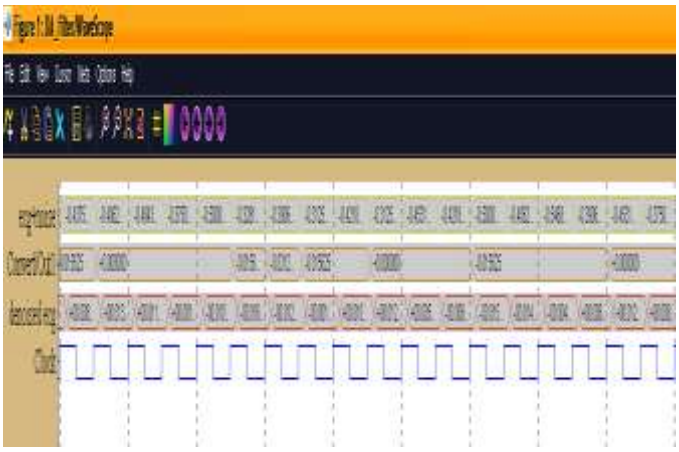

Fig. 8: Output waveforms for least square design

Fig.9: Results after Implementation on Spartan 3E Device.

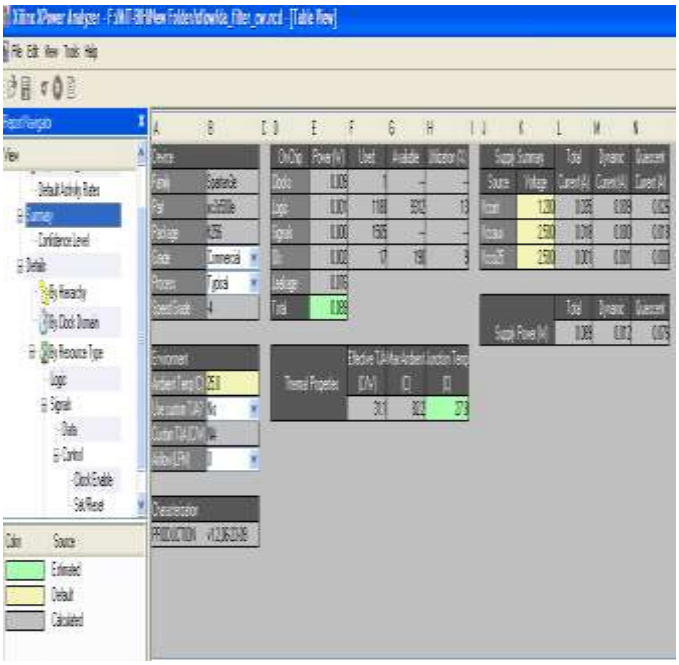

Fig.10: Snap shot of ISE Power analyzer generated from System Generator

Table 2 – Comparison of Hardware result between FPGA Spartan 3E and DSP device TMS320C64x [4].

Device	Constraints	FIR filter Design
Spartan 3E	Clock Rate	50 MHz
	Power Utilization(mW)	89
TMS320C64x	Clock Rate	400-1000 MHz
	Power Utilization(mW)	654-1303 mW

VI. CONCLUSION

This work is carried out for making solutions for power line interference from ECG noise signals. Noise cancellation from noisy ECG signal was explained clearly. FIR filter was chosen because of its simplified architecture & they are logically stable. This research work based on selection of filters and its implementation on FPGA device. Different types of FIR filters are designed like equiripple, least square and by windowing methods like Kaiser, Rectangular, Hamming, Hann, Blackman, and Bartlett for the removal of Powerline Interference from ECG signal.

On the basis of SNR at output and number of adders and multipliers required for the design equiripple and least square designs are chosen for the implementation on FPGA device. For final implementation of FIR filter on FPGA there are different techniques available like Canonic Signed Digit (CSD), Dempster-Mcleod (DM) LUT based, Constant Coefficient Multiplier (KCM) and Distributed Arithmetic (DA) method [8]. Out of these different methods Distributed arithmetic appears to be very efficient solution [9] for LUT-based FPGA architectures. Notch filters are designed using Distributed arithmetic technique and implemented on Spartan 3E FPGA device. It is observed from Table 2 that, FPGA is more efficient than DSP as it requires less power also observed in Snap shot of ISE Power analyzer generated from System Generator. Also better results have been observed for FPGA as compared to DSP for real time application [4] [5].

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