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Design a Low Power Built in Self-Test (BIST) Architecture for Fast Multiplier and Optimize in Terms of Real Time Functionality

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Abstract—Aiming low power during testing, May present a methodology for deriving BIST Architecture for fast Multipliers. In my propose Research several design rules for designing the Wallace tree in order to be fully testable under the cell fault model. The proposed low power BIST Architecture for the derived multipliers are achieved by: (i) Introducing Test Pattern Generators (ii) Properly assigning the TPGs outputs to the multiplier inputs and (iii) Significantly reducing the test vector length. In this work, I have implemented 4bit * 4bit Multiplier with many test pattern generators (TPG) alternative. A BIST TPG Architecture was use of 6 bit counter. I have calculated operation speed, time delay, area, power consumption for Design. Reduction of power dissipation achieved by properly assigning the TPG outputs to the multiplier inputs, significantly reducing the test set length, suitable TPG built of a 6-bit counter

Keywords-BIST(Built in self test), TPG(Test pattern generator), Wallace tree multiplier.

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I. INTRODUCTION

Design for testability techniques are design specifically employed to ensure that adevice is testable. Two important factor to testability are Controllability andObservability. *Controllability* is the ability to a specific signal value at each node ina circuit and control the output by setting values on the circuit's inputs. *Observability* is the ability to the signal value at any node in a circuit by control the circuit's inputs and observing its circuit’s outputs. The main features that they make it easier to develop and apply the device is manufacturing tests for the designed hardware. The purpose of manufacturing tests is validate that the product hardware contains no MANUFACTURING defects that could, otherwise, the product’s doesn’t correct functioning.[3]

A Built-In Self-Test (**BIST**) is a mechanism that permits amachine to test itself. Engineersdesign BIST to meet requirements such as: high reliability and lower repair cycle times orconstraints such as: limited technician accessibility and cost of testing during manufacture.[1]The main purpose of BIST is reduce the complexity, and decrease the cost andreduce reliance upon external test equipment. BIST reduce cost intwo ways: reduce test-cycle duration and reducethe complexity of the test setup.[2]Both lead to a reduction in charges for automated test equipment (ATE) service.BISTtechniques can be classified into two categories, namely on-line BIST, which includesconcurrent and non-concurrent techniques, and off-line BIST.[3]

The basic building blocks of arithmetic circuits in digital signal processing systems areregisters, multiplier and adders. In digital signal processing the significance of real timeincreases as do the requirements of the arithmetic capability of a signal processor.Multiplication is arithmetic operation in digital computer systems.Wallace tree multiplier,widely used as embedded cores in general-purpose data path structures and specialized digitalsignal processors, pose serious testability problems. In that multiplier partial productsaccording by using Wallace tree summation and carry look ahead addition.

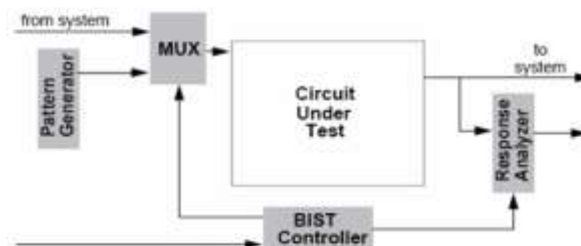

Fig.1 Basic BIST Architecture

Now a days we are using very high speed ICs and its external testing by fast multiplier core.In complex IC, lowcontrollability and observability of embedded blocks impose serioustestability problems. BIST is a design for testability (DFT) technique in which testing iscarried out using built in hardware features. Since testing is built into the hardware, it is fasterand efficient. BIST techniques are aimed at overcoming the problems and limitation ofexternal testing. In BIST scheme, the test patterns are generated and then applied to theCircuit under Test (CUT).The low power as a feature of a BIST scheme is a significant target due to quality as well ascost related issues. There are quality as well as cost related issues that make the powerdissipated during test application an important factor:

a) Reliability.
b) Technology.
c) Cost.[5]

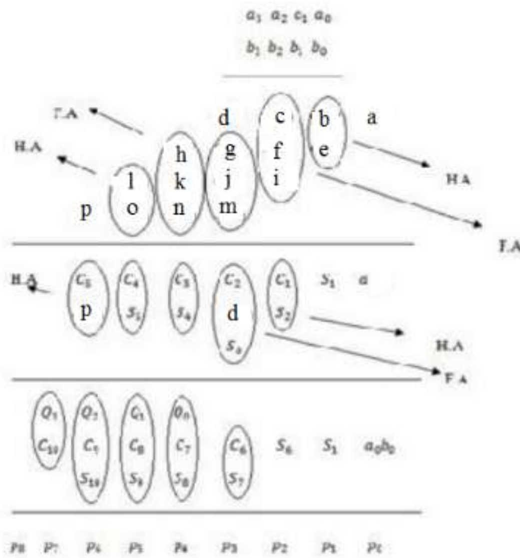

Fig.2 Wallace tree multiplier

II. TESTING FOR FAST MULTIPLIER

We consider m x n multipliers with inputs X (X3.......X0)and Y (Y3.....Y0). TPG proposed in [12] for such multipliers (seeFigure 3) consists of 6-bit counter whose 8 outputs are used to the multiplier inputs A and B. When A has 4 bit respectively B has also 4 bits. Multiplexers are used to select between normal inputs and BISTs inputs.The design of the Wallace Tree Unit can be done inseveral ways. The 256 vectors oftheir proposed TPG are capable of providing all possibleinput combinations to the inputs of every full or half addercell.They do not propose a specific method fordesigning the Wallace Tree Unit we could conclude thatthe above is valid no matter which structure is used for theWallace tree. However this conclusion is not correct. In[8] we have indicated several Wallace tree structures forwhich this does not hold. In other words, the Wallace treestructure must follow certain design rules in order for itscells to receive all possible input combinations. These design rules are:

- The partial product bits (PP bits) are grouped intriplets and summed at the first level of each Wallace tree.If the number of PP bits modulo 3 is non zero then theremaining PP bits are summed at next levels of theWallace tree along with carry bits.
- If a carry occurs the i-1 level of a certain Wallacetree, then this carry should be inserted at a level k adder ofthe succeeding most significant tree, such that k <i.
- Wallace tree has at most one half adderwhich either resides at the last or the previous to the lastlevel of the tree.
- The sign extension bits are summed either at thelast or the previous to the last level of each tree. In thelatter case a half adder should not be used.
- Carry bits that are the outcome of trees which sum alot of carry bits of less significance should be propagatethe highest possible level of the succeeding tree and ifpossible added with the outcome of subtrees that receiveonly a very small number of carry bits.We have verified the validity of these design rules byconstructing various multipliers (with operand sizes ofn = 8, 12, 16, 24, 32).

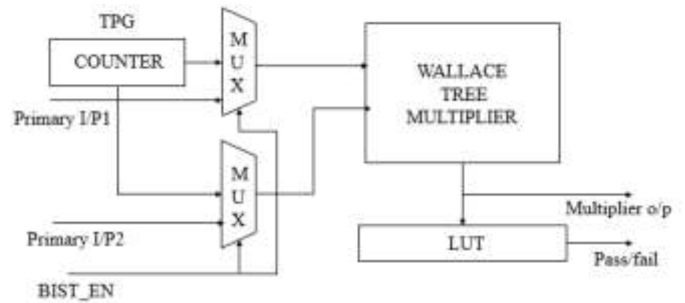

Fig.3 BIST Architecture for Fast Multiplier

After the description of the way fast multipliers can bedesigned to be easily testable under the 256 vectorsproduced by the basic BIST [6], we will focus in the nextsection on the production of a new BIST scheme takingalso the low power objective into account.

III. LOW POWER DURING FOR TESTING

Charging and discharging of capacitance is the dominant factor of power dissipation (denotedby P) in full static CMOS circuits [7], the dominant today technology. It has been reported that in high frequency CMOS circuits this accounts for at least 90% of the total powerdissipation. Denoting the power supply voltage by Vdd, the load capacitance at line l by Cl, andthe total number of transitions at line l by T(l), P can be formulated by:

$$P = (1/2)Vdd^2 \sum l Cl\, T(l) \ldots\ldots\ldots\ldots\ldots (1)$$

It is evident that the power dissipation can be reduced by reducing T(l). By reducing thenumber of transitions at the primary inputs of the circuit it is expected that the total number oftransitions at the lines of the circuit will also be reduced leading to lower power dissipation.However, depending on the circuit structure, the transitions at some primary inputs cause moretransitions at internal lines than those at other primary inputs. A procedure has been presented in for identifying those primary inputs that cause more transitions at internal lines.[5]

A. *Test Pattern Reduce*

It is well known that in BIST schemes some vectorsgenerated by the TPG circuits are not useful for testingpurposes. Therefore another way for reducing the powerdissipated during the test application is to reduce thenumber of vectors applied to the circuit under test.A straightforward approach to this problem is to use afault simulator along with a test set compression program.The result that would be obtained by this method wouldbe an optimal test set in terms of its cardinality but totallyinappropriate for implementation as a TPG circuit. This isbecause the vectors

that would be selected would have nostraight correlation between them. So for their generationa specially designed circuit would be required. Such circuitsapart from requiring large implementation area may alsodestroy any possible power dissipation gains attained bythe elimination of the original redundant test vectors.Another approach, that is not so straightforward, is tomodify the original TPG so as to only go through some ofits states. This solution does not guarantee to generate anoptimal number of test vectors but as long as the originalstate sequence is not disrupted a lot it can be implementedin approximately the same area as the original BIST TPG.We will follow the second approach. First we will tryto reduce the number of test vectors required forexhaustively testing the basic cells of the multiplier(aWallace tree full and halfadders) except for the CLA at the last stage. By using asimple simulator, we constructed a table with 256 rowsand X columns, with X indicating the number of cellsused in the multiplier. The content of each cell of the tableindicates the specific input combination that the specifictest vector applies to the corresponding cell of our design.The Gray encoding of the TPGdefine the order of the test vectors (rows in the table).Another ordering of the test vectors would lead to adifferent result.[8]

The next goal is to find a subset of rows in this table,able to apply all the input combinations at every cell. Since in our case the original TPG is a counter, this means that we must select large subsets of consecutive rows. We start by dividing the 256 rows into 8 groups of 32 consecutive vectors each.The idea behind this selection is that if a whole group of 32 vectors can be omitted, then this corresponds to the skipping of 4consecutive states of the 5-bit counter driving input B of the multiplier.

Table 1. Number of redundant groups vs group size for 8x8, 16x16 and 32x32 multipliers

Group Size	Number of groups	Number of redundant groups		
		8x8	16x16	32x32
32	8	0	1	0
16	16	6	5	6
8	32	20	20	18

Therefore it can be easily implemented without increasingsubstantially the area of the TPG circuit. Then, the sameprocedure is executed for groups of 16 or 8 vectors each.We stop at groups of 8 vectors since smaller groups wouldrequire a significant increase of the implementation areaof the TPG because this will destroy the Gray encoding onthe 3 least significant bits of the TPG. The above analysisleads to an area of the TPG vs power dissipation reductiontradeoff. For example for the 16x16 multiplier one canmake a selection between the removal of 1 group of 32vectors or the removal of 5 groups of 16 vectors (seeTable 1). The first solution will result in a smaller areaoverhead but will also lead to a smaller reduction in thepower dissipation.

Counter use as a test pattern generator generate the test vector. Forany of the bit generate test pattern and it's apply to any bit of the Wallace tree multiplier. FirstI'm using 8 bit counter for 4*4 multiplier. In 8 bit counter generate 256 vector but in this total vector some are reduce here may I explain which are vector discard first any of the one input multiply to zero output is always zero, in that 16 vector reduce. Second whenever any of the input is one is multiply to any of value that output is equal any of value, in that 15 vector discard. Third when N x M = M x N condition is satisfied than reduce the vector, in that 105 vector discard. Fourth using the gray code then reduce the half vector, in that reduce 60 vector.so in test length reduction finally generate the 60 vector its less than 256 vector. Test vector is directly proposed to power. When less test vector so low power dissipation. The test pattern generation requirements of BIST external testing strategies. External testing requires the fewest possible test vectors. Because they are stored in tester memory and often applied at low frequencies than the circuit operating frequency, a greater number of test vectors increases testing time and cost. In contrast, BIST test vectors must be highly regular so that small machines can generate them.

IV. RESULT

Whenever BIST_EN is active than multiplier inputs are counter's output and when multiplier output and lookup table output are equal than circuit is pass and when it's not equal than its fail. When after next BIST_EN is inactive than multiplier input are system input and when it's compare to lookup table and show the multiplier output.

Here show in figure 4 when BIST_EN is 0 then multiplier out is respect to system output and that time comparing path is disable so its 0.when BIST_EN is 1 then multiplier input is counter output and multiplier give the output and its check the lookup table and output is 1.and its fault free circuit.

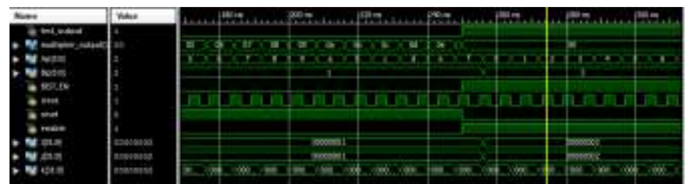

Figure. 4: Fault Free OUTPUT

Here show in figure 5 when BIST_EN is 0 then multiplier out is respect to system output and that time comparing path is disable so its 0.when in this multiplier forcefully apply to s4 =1'b1 and BIST_EN is 1 then multiplier input is counter output and multiplier give the output and its check the lookup table and output is 1 and then when not using s4=1'b1 then its output is wrong and multiplier output is wrong .and its fault circuit.

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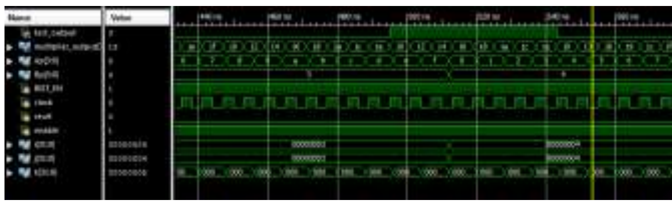

Figure.5: Fault OUTPUT

- Top module synthesis report

- Device utilization summary:

Selected Device: 7a100tcsg324-3

Slice Logic Utilization:

Number of Slice LUTs: 60 outof 63400 0%

Number used as Logic: 61 outof 63400 0%

Speed Grade: -3

Maximum combinational path delay: 10.861ns

Power (mw): 42.38mW

- Wallace tree multiplier report

- Device utilization summary:

Selected Device: 7a100tcsg324-3

Slice Logic Utilization:

Number of Slice Registers: 16 outof 126800 0%

Number of Slice LUTs: 11 outof 63400 0%

Number used as Logic: 11 outof 63400 0%

Speed Grade: -3

Minimum period: 1.412ns (Maximum Frequency: 708.366MHz)

Minimum input arrival time before clock: 1.142ns

Maximum output required time after clock: 0.640ns

Delay: 1.412ns

Supply Power (mW) : 42.38Mw

- Lookup table report
- Device utilization summary:

Selected Device: 7a100tcsg324-3

Slice Logic Utilization:

Number of Slice Registers: 24 outof 126800 0%
Number of Slice LUTs: 27 outof 63400 0%

Speed Grade: -3

Minimum period: 1.412ns (Maximum Frequency: 708.366MHz)

Minimum input arrival time before clock: 10.125ns

Maximum output required time after clock: 5.469ns

Maximum combinational path delay: 5.367ns

V. CONCLUSION

Wallace tree multiplier is used as embedded blocks in both general purpose data path structures and specialized digital signal processors. So by using this concept we can reduce the cost and power of the Design. Wallace tree Summation unit fully testable under the Cell Fault Model. In multiplier large number of combinational logic used so logic depth is large. If I am using scan techniques large number of test patterns are generate, so test time is high. When in BIST techniques reduce the test length so it's testable itself. Proposed architecture provides fault coverage larger than 99% for fault models.

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