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To Develop and Implement Low Power, High Speed VLSI for Processing Signals using Multirate Techniques

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Abstract:- Multirate technique is necessary for systems with different input and output sampling rates. Recent advances in mobile computing and communication applications demand low power and high speed VLSI DSP systems [4]. This Paper presents Multirate modules used for filtering to provide signal processing in wireless communication system. Many architecture developed for the design of low complexity, bit parallel Multiple Constant Multiplications operation which dominates the complexity of DSP systems. However, major drawbacks of present approaches are either too costly or not efficient enough. On the other hand, MCM and digit-serial adder offer alternative low complexity designs, since digit-serial architecture occupy less area and are independent of the data word length [1][10]. Multiple Constant Multiplications is efficient way to reduce the number of addition and subtraction in polyphase filter implementation. This Multirate design methodology is systematic and applicable to many problems. In this paper, attention has given to the MCM & digit serial architecture with shifting and adding techniques that offers alternative low complexity in operations. This paper also focused on Multirate Signal Processing Modules using Voltage and Technology scaling. Reduction of power consumption is important for VLSI system and also it becomes one of the most critical design parameter. Transistorized Multirate module which has full custom design with different circuit topology and optimization level simulated on cadence platform. Multirate modules are used AMI 0.6 um, TSMC 0.35 um, and TSMC 0.25 um technologies for different voltage scaling. The presented methodology provides a systematic way to derive circuit technique for high speed operation at a low supply voltage. Multirate polyphase interpolator and decimator are also designed and optimized at architectural level in order to analyze the terms power consumption, area and speed.

Keywords: *VLSI-Very large scale integrated circuit, VHDL-Very high speed hardware description language, DSP-Digital Signal Processing, FIR: Finite impulse response, FPGA: Field Programmable gate array, MCM-Multiple Constant Multiplication*

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I. INTRODUCTION:

The Multirate techniques are included to reduce the computational complexity. This Multirate design methodology is systematic and applicable to many problems. There are many reasons to change the sample rate of a sampled data signal. Multirate filters are interfaces of continuous & sampled data which results in a cost reduction components as well as improvement of signal quality. Much of the research effort of the past years in the area of digital electronics has been directed towards increasing the speed of digital systems. Recently, the requirement of portability and the moderate improvement in battery performance indicate that power dissipation is one of the most critical design parameters. The most important parameters to measure the quality of a circuit are area, delay and power dissipation while demanding high speed. Hence, in recent VLSI systems the power delay product becomes the most essential metric of performance. The presented methodology provides a systematic way to derive circuit technique for high speed operation at a low supply voltage. It is commonly accepted that low power circuits are very slow circuits and high speed circuits required very high power consumption. In many practical application of digital signal processing, there is a problem of changing the sampling rate of a signal, either increasing it or decreasing it by some amount [2][29]. Telecommunication system transmits and receives the different types of signals e.g. fax, speech, video etc. There is a requirement to process the various signals at the different rates with corresponding signals bandwidth. Digital audio engineering is an area that has benefited significantly from Multirate techniques. For example, it is used in the compact disc player to simplify the D/A conversion processes by maintaining the quality of the reproduced sound.

Need of Multirate DSP

A Discrete time system with unequal sampling rate at various part of the system is called Multirate system. Multirate digital signal processing is required in digital systems when more than one sampling rate is required. In digital audio, the various sampling rates used are 32 KHz for broadcasting, 44.1 KHz for compact disc and 48 KHz for audio tape. So, when audio professionals transfer recorded music to CDs, they need to do a rate conversion. Also, in digital video the sampling rate needed for composite video signals are 14.318 MHz for NTSC and 17.734 MHz for PAL. Both signals can be received in video receivers by sampling rate converter. But, the sampling rates for digital component of video signals are 13.5 MHz and 6.75 MHz for luminence and colour difference signal. Multirate signal processing is needed in digital transmission systems like teletype, facsimile and low bit rate speech where data is handled with different rates [28]. In speech processing, Multirate techniques are used to reduce the storage space or the transmission rate of speech data.

Basic Operations of Multirate DSP

In single rate system, only one sampling rate is used throughout a digital signal processing systems whereas in Multirate system the sampling rate is changed at least once. It is commonly used for audio and video processing, communication systems and transforms analysis. Different sampling rate can be obtained by

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using upsampler and downsampler [3]. An Upsampler increasing the rate of previously sampled signal. When Up sampling is performed on sequence of samples of a continuous function or signal then it produces an approximation of the sequence which obtained by sampling the signal at higher rate. A downsampler decreasing the rate of previously sampled signal. The basic operations in Multirate processing to achieve this are Decimation and Interpolation.

Multirate Polyphase Filter Structure

Polyphase is a way of doing sampling rate conversion that leads to very efficient implementations. Sampling rate reduction is required for efficient transmission and a sampling rate increase is required for the regeneration of the speech. It can be efficiently implemented using finite impulse response digital filters. It is found that efficient implementations of low pass FIR filters could be obtained by a process of reducing the sampling rate, filtering and increasing the sampling rate to the original frequency [28]. FIR based filtering is advantageous in many digital signal processing systems due to the possibility of exact linear phase and freedom of stability problems. Multirate technique is used in acquisition of high resolution spectral analysis and the design and implementation of narrowband digital filtering.

Polyphase Implementation of Decimator

The problem of designing Multirate Polyphase Interpolator & Decimator has received a great attention due to large number of multiplications. Decimator is utilized to decrease the sampling rate. The decimator consists of an anti-aliasing filter and a down sampler by a factor M depicted in Figure below,

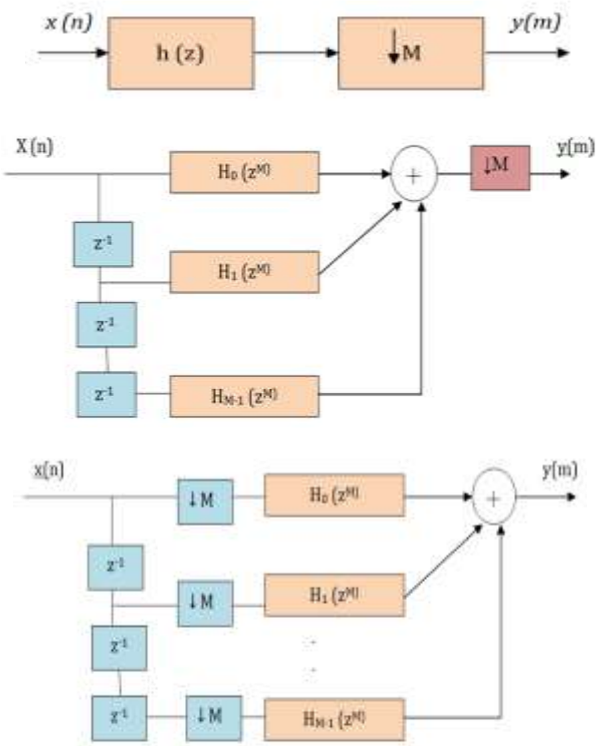

Figure 1 Polyphase Representation of Decimator

Polyphase Implementation of Interpolator

Polyphase implementation of interpolator focused that some of the delay line samples in an interpolator are zero valued. In this case the rate expander is removed to eliminate the need to store zero valued samples. In this approach, for each input samples fed into the delay line, the N/L delay line samples are used to compute L output samples with each samples computed with a different set of filter coefficient [22].

Telecommunication system transmits and receives the different types of signals. There is a requirement to process the various signals at the different rates with corresponding bandwidth. The role of a filter in decimation and interpolation is to suppress aliasing and to remove imaging. Digital Signal Processing has become essential to the design and implementation of high Performance audio, video, multi-media and communication systems. The efficiency of FIR filters for sampling rate conversion is improved using the Polyphase realization. Filtering is embedded in the interpolation process and polyphase structure is used to achieve the interpolation by a given factor at a low data rate.

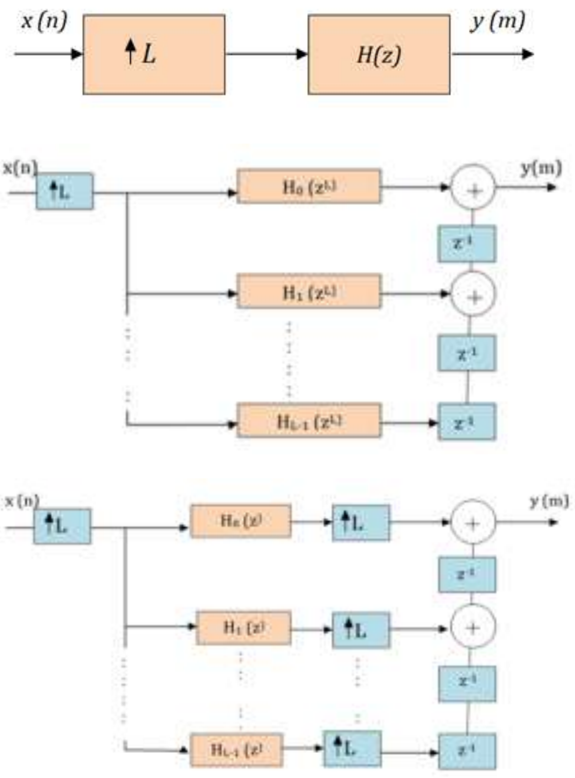

Figure 2 Polyphase Representation of Interpolator

II. DESIGN METHODOLOGY:

Basic Concept of Improvement

The presented methodologies have been divided into three phases wherein in first phase, Transistorize Multirate module which has top level full custom design approach is developed with voltage and technology scaling. In second phase, area, power and speed efficient techniques for Multirate FIR filter using MCM-digit serial architecture with shifting-adding

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concept which offer alternative low complexity in operations and improved the parameters is presented. In third phase, an efficient method has been presented to implement low power, high speed Multirate Polyphase Interpolator & decimator which applicable in wireless communication systems. Direct form, transpose form and combination of MCM-digit-serial adder is suggested which offer low complexity designs, occupy less area, low power consumption maintaining higher speed.

CMOS Dynamic Logic Circuit Techniques

Designing a CMOS dynamic circuit using a low supply voltage for the next generation CMOS VLSI is a challenge. CMOS dynamic logic circuit techniques have been used to enhance the speed performance of VLSI systems. The high speed design using Multirate approach increases the speed to a great extent but it increases the hardware complexity [26].

Design of Transistorize Multirate Module

Transistorize Multirate module which has top level full custom design approach is developed with different circuit topology and optimization level. The new approach is used to reduce the complexity in the design to improve the essential parameters. The basic modules of Multirate signal processing are designed and verified its coefficients by the voltage and technology scaling. Upsampler consist of Shift register, D F/F and Multiplexer whereas downsampler consist of D F/F, clock generator and multiplexer. Scaling process has been done then it is simulated and synthesized on cadence platform. Obviously, some techniques applied to high speed circuits needed larger power consumption. However, it is directed that many techniques are used to reduced power dissipation in high speed circuits. Reduction of power consumption is important for VLSI system and also it becomes one of the most critical design parameter. The basic Multirate modules are depicted as below,

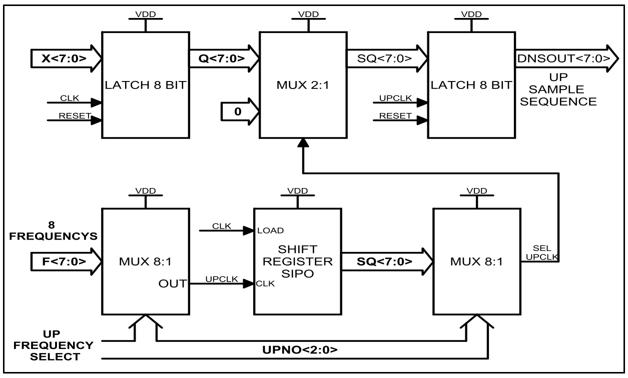

Figure 3 Block Diagram representation of Upsampler

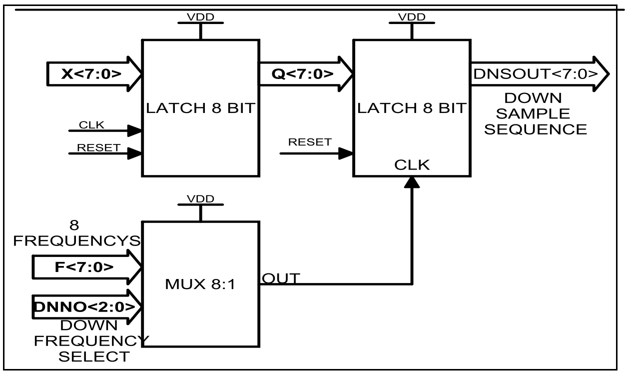

Figure 4 Block Diagram Representation of Downsampler

Concept of Improvement in Power Dissipation and Speed in CMOS Devices

The VLSI architecture can performed DSP function at M times slower operating frequency while retaining same data throughput rate. This feature can help achieve significant power saving under low power voltage without loss of speed performance [35].Power dissipation in CMOS circuit is given using following equation

$$P= \alpha. C_{eff} . V_{dd}^2.F_{clk} \quad (1)$$

Delay of CMOS device can be approximated as

$$TD= C_L.V_{dd}/I \quad (2)$$

$$TD=C_L.V_{dd} /\varepsilon (V_{dd}-V_t)^2 \quad (3)$$

Equation plays the essential role in low power VLSI design. Now, CMOS Feature size has been reduced to smaller transistor size improved the device/circuit speed performance and reduces the total silicon area, hence total power consumption reduced [25]. Reduction of the future size is another commonly used approach which achieves low power consumption at technology level. Delay of the circuit is inversely proportional to $(V_{dd}-V_t)^2$. Thus, it is desirable to reduce the magnitude of V_t either to minimized the degradation of speed caused by lowered V_{dd} or to allow further reduction in V_{dd}. Compared with other approaches architectural low power design is one of the most economical way to save power. In this paper, a new techniques Multirate approach is presented to compensate speed penalty for low power design. At the same, it can be used for high speed design as well [26].

Highly Efficient Architecture Techniques

FIR Filter Design Styles

Finite impulse response (FIR) filters are of great importance in digital signal processing systems since their characteristics in linear phase and feed forward implementations make them very useful for building stable high performance filters. The direct and transpose form FIR filter implementation can be

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made. Although, both architectures have similar complexity in hardware, the transposed form is generally preferred because of its higher performance and power efficiency [10].

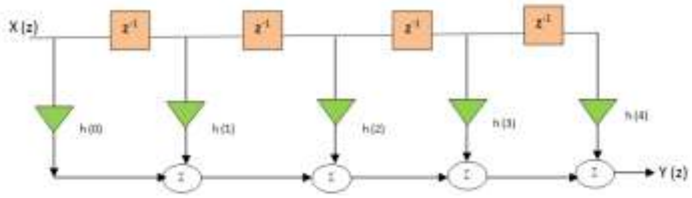

Figure 5 Direct Form of FIR Filter

MCM-Shift-Add Techniques

The multiplier block of the digital FIR filter in its transposed form is shown, where the multiplication of filter coefficients with the filter input is realized and it has significant impact on the complexity and performance of the design because a large number of constant multiplications are required[11], [15] .

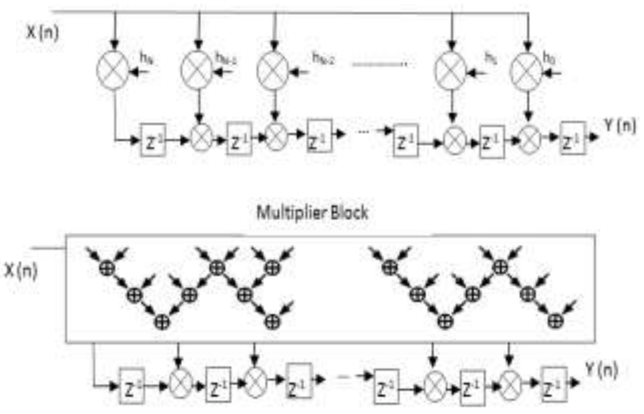

Figure 6: FIR Filters Implementations (a) Transposed Form with Generic Multipliers (b) Transposed Form with MCM Block

Hence, the multiplication of filter coefficients with the input data is implemented under shift-adds architecture, where each constant multiplication is realized using addition/subtraction and shift operations [17].

As a small example, suppose the multiplication of multiple constants 11 and 13 by the variable x. Observe from Figure 7 (a) that the multiplierless implementation without partial product sharing requires four operations.

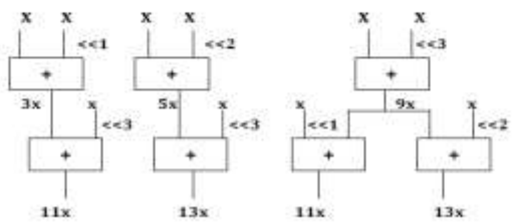

Figure 7: The shift-add implementations of constant multiplications 11x and 13x a) without partial product Sharing b) with partial product sharing.

However, the sharing of partial product 9x in both multiplications reduces the number of required operations to 3 as given in Figure 7(b).In the last two decades, many efficient algorithms have been proposed for the optimization of the number of operations in MCM. These methods can be categorized into the Common Sub expression Elimination and the graph-based algorithms [16].

Another concept can be used to optimize the parameters is multiplication using shift, additions and subtractions realization without general multipliers. The number of additions and subtractions can be significantly reduced by using common partial results [17]. As additions and subtractions have similar complexity as an example, consider the constant multiplications 29x and 43x. Observe from Figure that the sharing of partial products 3x and 5x reduces the number of operations from 6 to 4. The decompositions of 29x and 43x in binary are listed as follows:

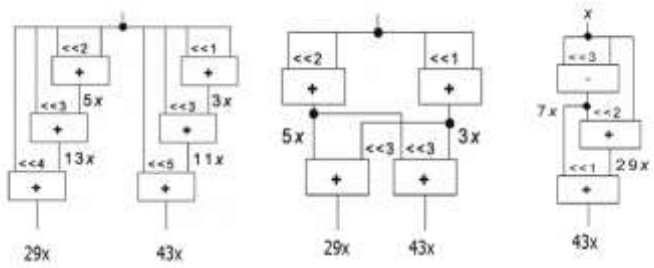

Figure 8: Shift-adds implementations of 29x and 43x (a) Without partial product sharing and with partial product sharing (b) Exact CSE algorithm (c) Graphic Based algorithm

Digit Serial Architecture Method

Another method which requires moderate sample rate, these systems may be ineffective. Bit serial system will be too slow and bit parallel system is faster. Therefore, digit serial systems have become attractive for digital designers in the recent years. These systems process multiple bits of the input word, referred to as the digit size in one clock cycle. For a digit size of unity, the system reduces to a bit serial and for a digit size equal to the word length the system reduces to a bit parallel system. Most of the DSP computations involve the use of multiply accumulate operations. Therefore, the design of fast and efficient multipliers is imperative [17], [18]. The bit serial systems which process one bit of the input sample in one clock cycle are area efficient and ideal for low speed applications. On the other hand, bit parallel systems which process one whole word of the input sample in one clock cycle are ideal for high speed application.

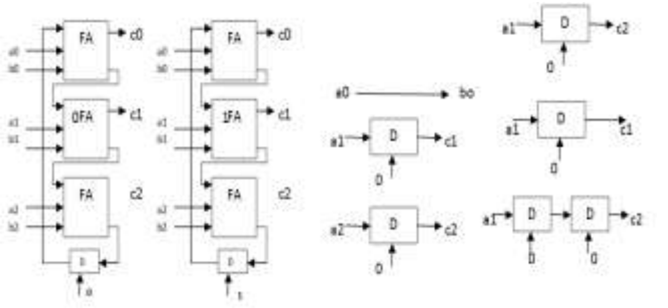

Figure 9: The digit serial operation when d is equal to 3 (a) Addition operation (b) Subtraction Operation(c)Left shift by 2 times (d)Left shift by 4 times

In digit serial arithmetic, data words are divided into digits with a digit size of d bits which are processed in one clock cycle. The special cases of the digit serial computation called bit serial and bit parallel processing occur when the digit size d is equal to 1 and input data word length respectively. The digit serial computation plays an important role when the bit serial implementations cannot meet delay requirements and the bit parallel designs require excessive hardware. Thus, an optimal tradeoff between area and delay can be obtained by changing the digit size parameter (d). The digit serial addition, subtraction, and left shift operations are depicted in Figure when d is equal to 3. Figure 9(a) shows that a digit serial addition operation required the number of full adders (FAs) is equal to d and the number of necessary D flip-flops is always 1. The subtraction operation is shown in Figure 9(b) which is implemented using 2's complement requiring the initialization of the D flip-flop with 1 and additional d inverter gates with respect to the digit-serial addition operation. In a left shift operation figure 9(c)-(d), the number of required D flip-flops is equal to the amount of shift.

Figure below illustrates the bit-serial implementation of 29x and 43x obtained from Figure 8 (c).

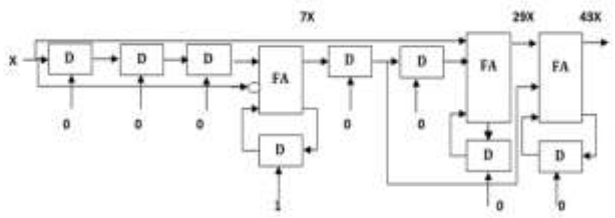

Figure 10: Bit-serial realization of shift-adds implementation of 29x and 43x

The network includes 2 bit serial additions, 1 bit-serial subtraction, and 5 D flip-flops for all the left shift operations. Observe from Figure that at each clock cycle, one bit of the input data x is applied to the network input and one bit of the constant multiplication output is computed [16]. Note that the digit-serial design of the MCM operation occupies significantly less area when compared to its bit-parallel design and the area of the design is not dependent on the bit-width of the input data. However, the latency of the MCM computation is increased due to the serial processing. Suppose that x is a 16-bit input value. To obtain the actual output of 29 x and 43 x in the bit-serial network of Figure, 21 and 22 clock cycles are required respectively1. Thus, necessary bits must be appended to the input data x, i.e., 0s, if xis an unsigned input or sign bits, otherwise. Moreover, in the case of the conversion of the outputs obtained in digit-serial to the bit parallel format, storage elements and control logic are required. Note that while the sharing of addition/subtraction operations reduces the complexity of the digit-serial MCM design, the sharing of shift operations for a constant multiplication reduces the number of D flip-flops, and consequently, the design area. Observe from Figure that two D flip-flops cascaded serially to generate the left shift of 7x by two can also generate the left shift of 7x by one without adding any hardware cost.

III. EXPERIMENTAL RESULTS

Phase-I: Transistorize Module of Upsampler

The Transistorized module of Upsampler is designed using Multirate signal processing approach by Cadence software and analyzed the parameters on voltage & technology scaling. It is depicted in figure below, AMI 0.6 µm, TSMC 0.35 µm and TSMC 0.25 µm technologies are used to improve the parameters.

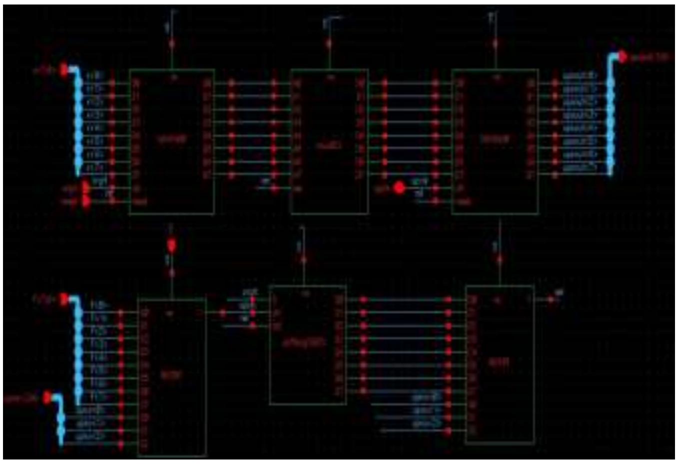

Figure 11 Transisterize Circuit Diagram of Upsampler

Testing results are observed at various supply voltages which found satisfactory. The comparative analysis of the essential parameters at different technologies of basic Multirate module is specified in table below,

Tech	AMI 0.6µm		TSMC 0.35µm		TSMC 0.25µm	
V	Speed GHz	Power nW	Speed GHz	Power nW	Speed GHz	Power nW
1v	0.1558	0.0501	1.2730	0.0124	0.5512	0.0211
2v	0.3254	0.0772	0.7981	0.0317	1.8478	0.0583

Table 1 Result of Transistorized Module of Upsampler

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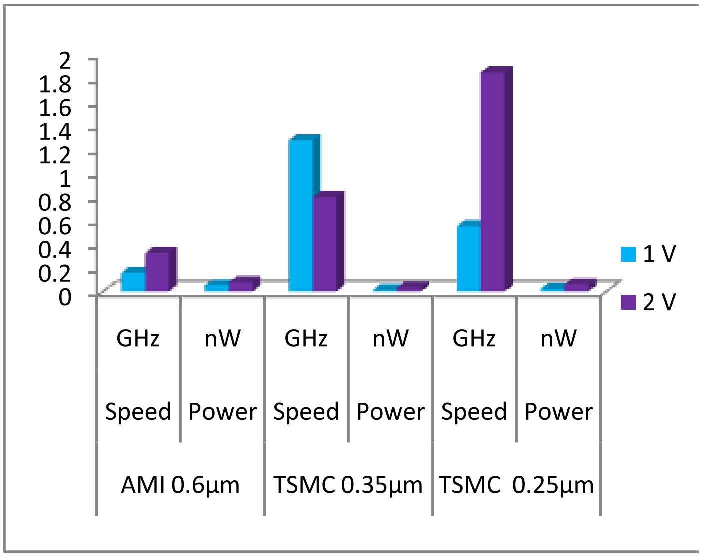


Graph 1 Speed-Power Improvement Graph

It is observed that TSMC 0.35µm technology at 1 V supply voltage required less power dissipation maintaining higher speed and TSMC 0.25 µm technology at 2V supply voltage maintaining higher speed at very less power dissipation. It is concluding that TSMC 0.35 µm and TSMC 0.25 µm improved the performance of the Multirate modules.

Transistorized Module of Downsampler

Transistorized module of Downsampler is designed using Multirate signal processing approach by Cadence software and analyzed the parameters on voltage & technology scaling. AMI 0.6 µm, TSMC 0.35 µm and TSMC 0.25 µm technologies are used to improve the parameters of Multirate modules.

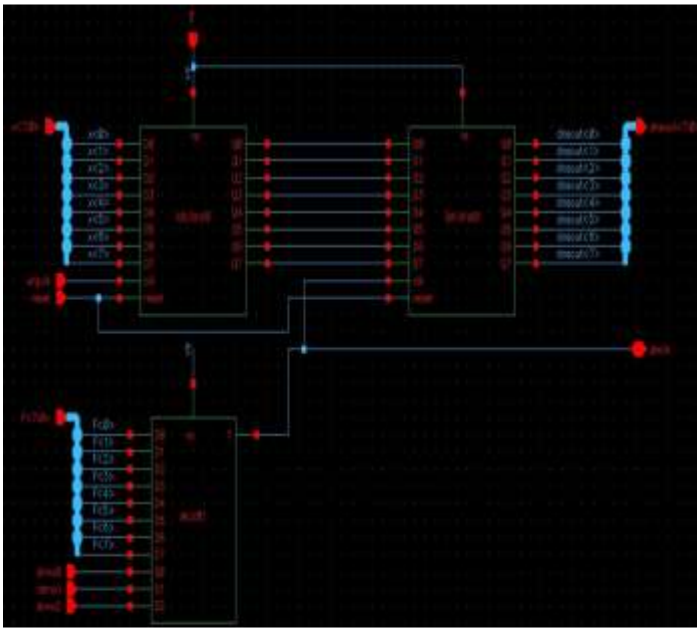
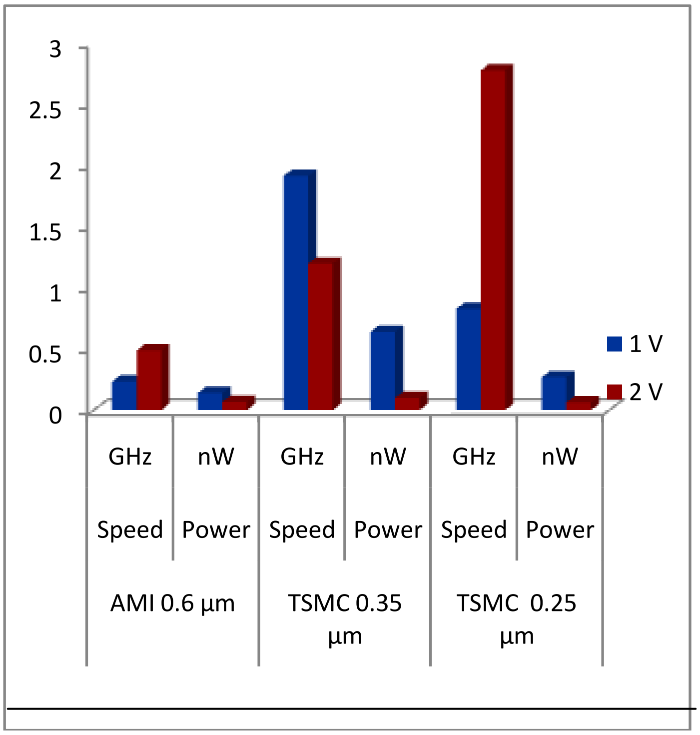


Figure 12 Transisterize Circuit Diagram of Downsampler

Testing Results and Comparative analysis of the essential parameters at of basic Multirate module at different technologies is specified in table below,

Tech	AMI 0.6 µm		TSMC 0.35 µm		TSMC 0.25 µm	
V	Speed GHz	Power nW	Speed GHz	Power nW	Speed GHz	Power nW
1v	0.2337	0.1404	1.9093	0.64	0.8267	0.27
2v	0.4882	0.0673	1.1972	0.099	2.7716	0.063

Table 2 Testing Result of Transistorized Module of Downsampler



Graph 2 Speed-Power Improvement Graph

It is observed that TSMC 0.35 µm technology at 2 V supply voltage required less power consumption maintaining higher speed and TSMC 0.25 µm technology at 2V maintaining higher speeds at very less power. Therefore, this technique is very efficient to improve the circuit parameters.

Phase-II: Multirate FIR Filter Design

Multirate FIR filter is designed using new techniques to improve the parameters and to avoid circuit complexity. Multiplier, adders and latches are reduced by different logic due to which power and area in system is reduced at great extend maintaining higher speed. Design results are verified using FPGA Cyclone–II Kit. The attention has been given to the MCM-digit serial architecture with shifting & adding technique that offers alternative low complexity in operations and improved the parameters. The Efforts are directed towards reduction of power and area at great extend succeeded by using multiple constant multiplier with combination of digit-serial adder block. In presented design constant multiplier block uses

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shift-add techniques. Shift unit does not consume any area therefore total cell area is reduced. Similarly, the area of adder block is reduced by digit-serial architecture. Earlier design uses 32 full adders but this technique required only two adders. So, it is most efficient technique which reduced power consumption and area by large value maintaining higher speed.

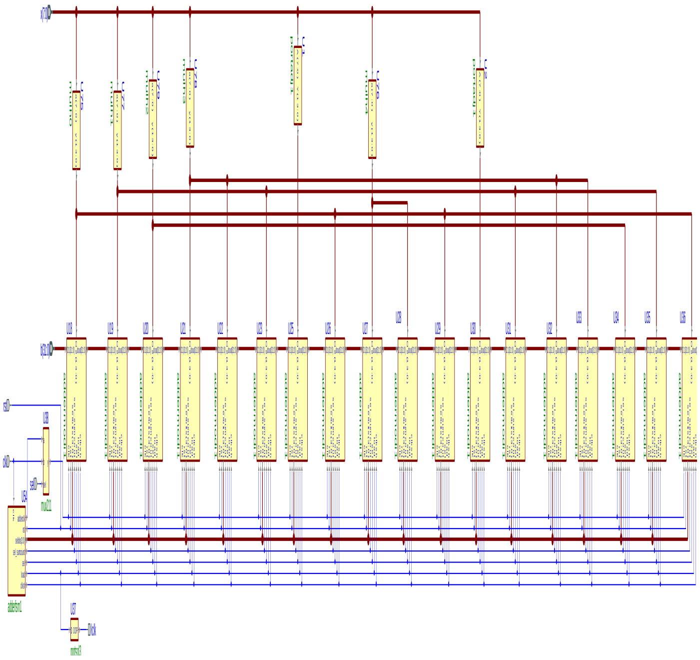


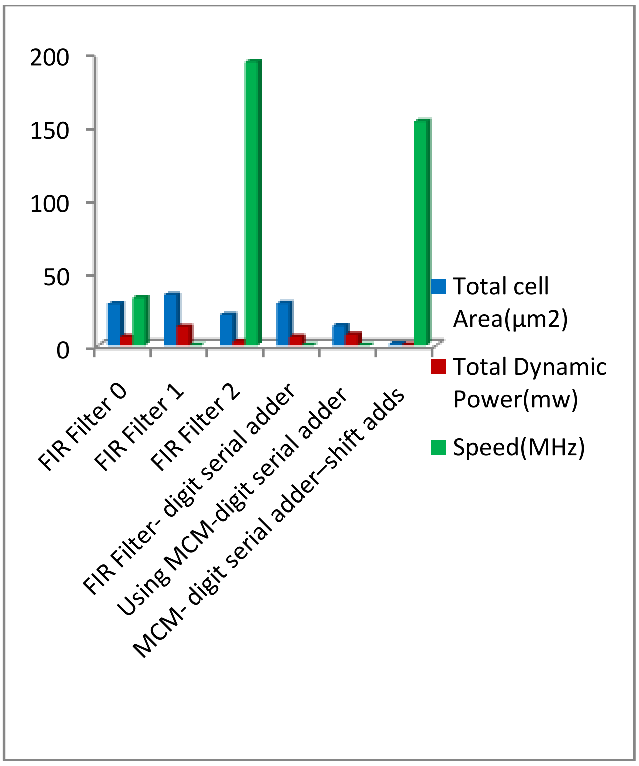
Figure 13 RTL View of FIR Filter using MCM-Digit Serial Adder-shift-adds Concept

Filter Name	Combinational Area(μm^2)	Non-combinational Area(μm^2)	Total Cell Area (μm^2)	Cell Internal Power (mw)	Net Switching Power (mw)	Total Dynamic Power (mw)
FIR Filter 0	27050.4519	1404.14563	28454.5976	3.4263	2.4014	5.827
FIR Filter 1	29009.7793	5616.58252	34626.3618	7.7737	5.0117	12.78
FIR Filter 2	15383.1843	5616.58252	20999.7668	1.4735	0.87152	2.345
FIR Filter-digit serial adder	27431.9929	1404.14563	28836.1385	3.5082	2.3820	5.890
Using MCM-digit serial adder	13273.2121	151.114597	13424.3267	4.2176	3.0952	7.312

Table 3 Testing Result of Multirate FIR Filter with Various Techniques

Filter Name	Total cell Area(μm^2)	Total Dynamic Power	Speed
FIR Filter 0	28454.59761	5.8277 mW	32.624MHz
FIR Filter 1	34626.36188	12.7854 mW	-
FIR Filter 2	20999.76688	2.3450 mW	194.666MHz
FIR Filter- digit serial adder	28836.13853	5.8902 mW	-
Using MCM-digit serial adder	13424.32676	7.3128 mW	-
MCM- digit serial adder–shift adds	**988.815092**	**0.14922 mW**	**153.794MHz**

Table 4 Testing Result of High Speed Multirate FIR Filter with New Technique



Graph 3 Area-Power-Speed Improvement Graph

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Figure 14 Verification of Result 1111011 of Multirate FIR Filter

Phase III: Multirate Polyphase Decimator

Finally, an efficient method has been proposed to improve the parameters of Multirate Polyphase decimator applicable in wireless communication systems. MCM and digit-serial adder offer low complexity designs, occupy less area, low power consumption maintaining higher speed. Testing results have shown the efficiency of the proposed technique and the analysis of different architecture.

The Multirate Polyphase Decimator is implemented on FPGA cyclone –II device which shown complete setup of the design as shown in figure below

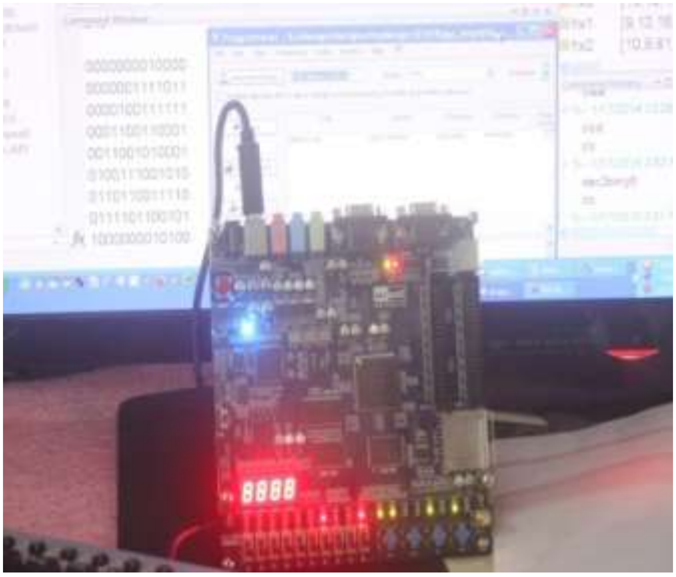
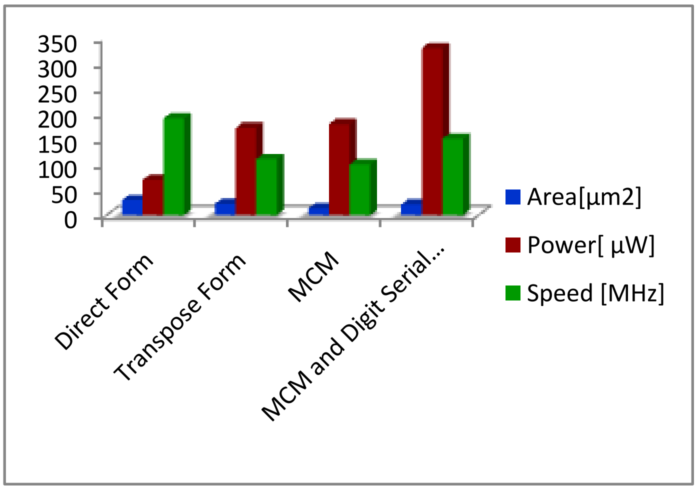


Figure 15 Verification of Result 10011100101 of Multirate Polyphase Decimator

Result: Multirate Polyphase Decimator

Type	Area[μm^2]	Power [µW]	Speed [MHz]
Direct Form	29741	70	190.621
Transpose Form	22579	173	111.025
MCM	13256	180	100.604
MCM and Digit Serial Adder	21271	330	151.579

Table 5 Testing Result of Multirate Polyphase Decimator with Various Techniques



Graph 4 Area-Power-Speed Improvement Graph

Multirate Polyphase Interpolator

An efficient method has been proposed to improve power dissipation, area and speed of Multirate Polyphase Interpolator. MCM- digit-serial adder occupies less area, low power consumption maintaining higher speed. Testing results have shown the efficiency of the proposed technique and the analysis of different architecture.

Filter Structure	Area[μm^2]	Power (µw)	Speed (MHz)
Direct Form	31921	113	205.634
Transpose Form	37511	222	106.315
Using MCM	14747	220	103.189
Using MCM and Digit Serial Adder	23178	413	151.579

Table 6 Test Result of Multirate Polyphase Interpolator with various techniques

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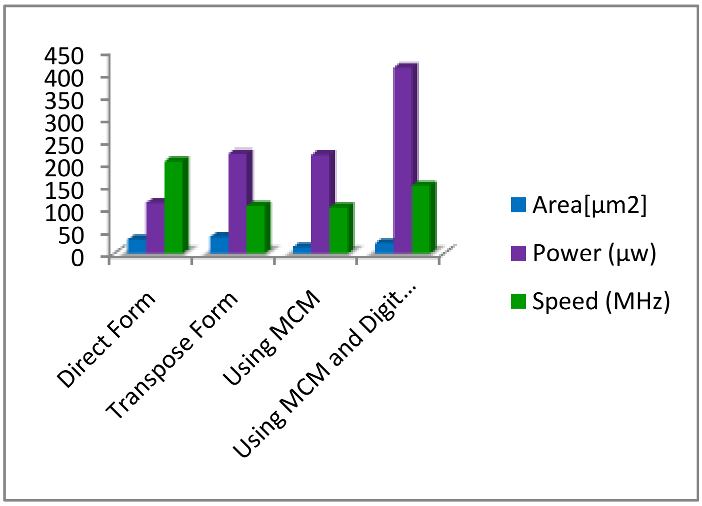

Graph 5 Area-Power-Speed Improvement Graph

IV. CONCLUSION:

This presented work has developed architecture technique and recent technology concept to improve the parameters of Multirate DSP modules. To open new possibilities of the Multirate modules using technology and voltage scaling the important parameters area, power dissipation and speed has been observed. Recent transistor technologies have chosen an optimal configuration in Multirate DSP modules. Top level system design approach is applicable which has given full custom design with different circuit topology. AMI 0.6 µm, TSMC 0.35 µm and TSMC 0.25 µm technologies are used to determined and improved the essential parameters of Multirate modules**.** From the testing results, it is observed that TSMC 0.35 µm technology at 1V supply voltage required less power dissipation maintaining higher speed and TSMC 0.25 µm technology at 2V supply voltage maintaining higher speeds at very less power. This Research methodology improves a speed and power dissipation of the system. Then the Multirate FIR filter is designed in direct form, transpose form, using MCM, using MCM-digit serial architecture and the fifth approach is to use combination of MCM-digit serial architecture with shifting–adding techniques to avoid circuit complexity. In the paper, attention has been given to the MCM-digit serial design with shift-add techniques that offer alternative low complexity in operations and improved the parameters. The complete design results are verified using FPGA. In a Final phase, module of Multirate polyphase Interpolator and Decimator has presented with newly developed approach. These modules are designed with four different approaches that are in direct form, transpose form, using MCM and using MCM-digit serial architecture with shift–add techniques to avoid circuit complexity. Improvement in the parameters is obtained using MCM and digit serial adder technique to a great extent and overcome problem of complexity & design performance. Direct form of Multirate Polyphase Interpolator and decimator is best suited for implementation of DSP system which requires very less power dissipation maintaining higher speed. The complete results are verified using FPGA. Multiple Constant Multiplications is efficient way to reduce the number of addition and subtraction in polyphase filter implementation. The presented techniques can be implemented in any real time applications in communication systems, speech and audio processing system, antenna and radar systems where more than one sampling rate is required and limited resources such as battery power, small space, restricted Speed etc.

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