A Review on Design and Development of Pipelined Quaternary Adder for Fast Addition

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***Abstract*—** The Binary logic circuits design is limited by the requirement of number of interconnections which increases the chip area with increase in logic. Arithmetic circuits play a very critical role in both general-purpose and application specific computational circuits. This paper presents the design of a multiple-valued half adder and full adder circuits. The proposed adders are implemented in Multiple-Valued voltage-Mode Logic (MV-VM*L)* and investigate the effect of one parameter on another. Quaternary (Four-valued) logic also provides easy interfacing to binary logic because radix 4 allows for the use of simple encoding/decoding circuits. The functional completeness is proved by a set of fundamental quaternary cells and the collection of cells based on the Supplementary Symmetrical Logic Circuit Structure (SUSLOC). Designing this adder using QSD number representation allows fast addition/subtraction which is capable of carry free addition and borrows free subtraction because the carry propagation chain are eliminated, hence it reduce the propagation time in comparison with radix 2 system.

Keywords:- *Half Adder, Full Adder FPGA, VHDL.*

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I. .INTRODUCTION

Due to the increase in the density of the very large scale integrated (VLSI) circuits is the result of advanced Integrated Circuits (IC) fabrication processes and the progress of automated design tools. When the number of devices accommodated on VLSI chips increases, many problems arise.

Arithmetic operations are widely used and play important role in various digital systems such as computers and signal processors. Modern computers are based on binary number system (radix =2). It has two logical states '0' and '1'. In such system, '1' plus '1' is '0' with carry '1' (i.e. 1+1=10). This carry should have to add with another '1', as a result further carry '1' generates. This creates the delay problem in computer circuits. So to get rid of this carry formation again and again signed digit is essential.

Depending upon the radix number R, the number system are named as ternary (R = 3), quaternary (R = 4) etc. arithmetic operations still suffer from known problems including limited number of bits, propagation time delay and circuit complexities. In QSD number system carry propagation chain are eliminated which reduce the computation time substantially, thus enhancing the speed of the machine.

Addition process is faster in QSD but the hardware circuitry will be complex due to more number of bits are required to encode the QSD number which ranges from -3 to +3. We propose a high speed QSD arithmetic logic design unit which is capable of carry free addition, borrow free subtraction, division, up-down count multiplications.

The paper is structured as follows: In Section II Literature review is explained. The Section III presents the proposed work with individual module. In Section IV we provides the conclusion part.

II. .LITERATURE REVIEW

Alejandro F. González [3] presents a fully integrated implementation of a multivalued-logic signed-digit full adder circuit using a standard 0.6- m CMOS process. A new prototyping technique for circuits that combine MOS transistors and NDR devices. In MOS-NDR, the folded current–voltage characteristics of NDR devices such as resonant-tunneling diodes (RTDs) are emulated using only nMOS transistors.

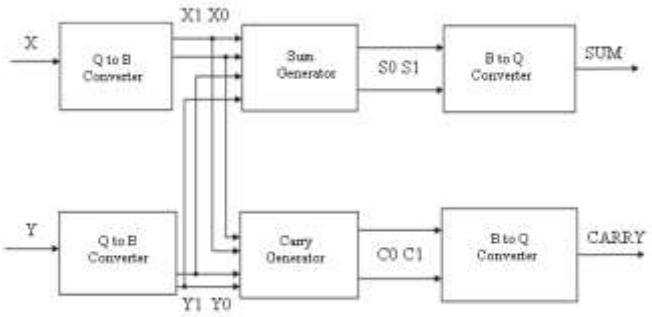
Dr. Amer Abu-Ali [4] presents special design for analog voltage-to-4 valued logic converter is implemented. In this study 2- bits converter was developed and tested using PLA (Programmable Logic Arrays) and two Digital to Analog converters.

Vasundara Patel K S [7] presents the design of half adder and full adder. The proposed adders are implemented in Multiple-Valued voltage-Mode Logic (MV-VM*L)*. The design is targeted for the 0.18 µm CMOS technology and verification of the design is done through HSPICE and COSMOSCOPE Synopsis Tools.

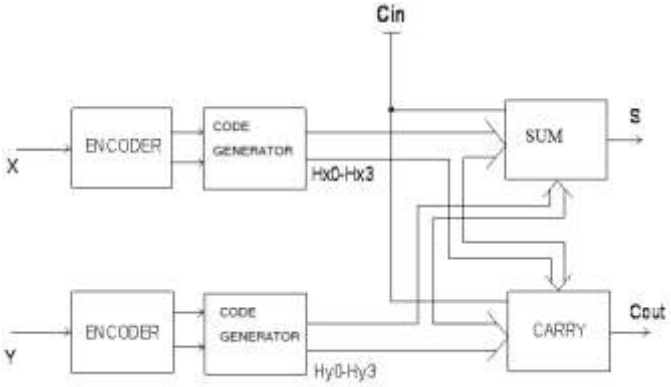
Ankita.N.Sakhare [8] Quaternary converter circuits are designed by using down literal circuits. Arithmetic operations like addition and multiplication in Modulo-4 arithmetic are per-formed by using multi-valued logic (MVL).Logic design of each operation is achieved by reducing the terms using Karnaugh diagrams, keeping minimum number of gates and depth of net in to consideration. The proposed circuit is Galois addition and multiplication which requires fewer gates. Simulation result of each operation is shown separately using Tspice.

III. PROPOSED WORK

The proposed work can be divided into the following parts,
Module 1. Development of Quaternary Half Adder
In this module, we would be developing a Quaternary Half adder circuit, which would perform addition of 2 quaternary numbers



Module 2. Development of Quaternary Full Adder
In this module, we would be developing a Quaternary Full adder circuit, which would perform addition of 2 quaternary numbers



Module 3. Development of Q to B and B to Q Converter
In this module, Quaternary to Binary and Binary to Quaternary Converters would be developed

Module 4. Development of Encoder Circuit
In this module, the proposed encoder circuit would be developed, which would be responsible for encoding the input data into proper Quaternary format

Module 5. Development Sum and Carry Block
In this module, the proposed Sum and Carry blocks would be developed, which would be responsible for adding the input data's and producing the proper outputs. The blocks would be developed with proper pipelining technique, so that the speed of the system can be optimized

Module 6. System integration with optimization
In this module, we would be integrating the entire system and forming the proposed adder would be developed and tested for various input combinations.

IV. CONCLUSION

Quaternary half adders are designed using binary logic gates and radix converters. Quaternary half adder requires only 76 transistors and dissipates 112µW of power at 1GHz. Quaternary full adder is designed with down literal circuit, code generators, Sum and Carry blocks which requires 148 transistors and dissipates 84µW at 250MHz.

Selection of different representation for the quaternary input in binary has reduced the requirement of the more hardware which enables to implement high performance quaternary full adder. These circuits consume less number of transistors and shows high performance. Consequently, this design is appropriate to be applied for construction of a high performance

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