Minimization of Latency and Power for Network-on-Chip

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***Abstract*—**Network-on-chip (NoC) has emerged as a imperative aspect that determines the performance and power consumption of many-core systems. This paper proposes a combination scheme for NoCs, which aims at gaining low latency and low power consumption. In the presented combination scheme, a peculiar switching mechanism, called virtual circuit switching, is proposed to interweave with circuit switching and packet switching. Flits traveling in virtual circuit switching can pass through the router with only one stage. In addition, multiple virtual circuit-switched (VCS) connections are granted to share a common physical channel. Moreover, a path allocation algorithm is used in this paper to determine VCS connections and circuit-switched connections on a mesh-connected NoC, such that both communication latency and power are optimized.

Keywords: *Network-on-chip (NoC), virtual channel allocation (VA), route computation (RC), circuit-switched (CS), virtual circuit switch (VCS), packet-switched (PS), switch allocation (SA), switch traversal (ST).*

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I. INTRODUCTION

With the fast development of progressive nanometer IC technology, continuously rejecting transistor dimensions allow designers to integrate an increasing number of processors or IP cores into a single chip. Classical bus-based communication is no longer applicable due to its poor scalability. Rather, network-on-chip (NoC) has emerged as a scalable and promising solution to global communications within large multicore systems. Typical examples are the
48-core SCC processor [1], the 64-core Tile64 chip multiprocessor [2], and the 80-core Tera FLOPS research chip [3]. All these examples exploit packet-switched (PS) NoCs, which bring the advantage of high flexibility and high bandwidth to communications. However, such merit is achieved by exploiting a complex router pipeline. The pipeline stages of a baseline PS router include the buffer
write (BW) stage, the route computation (RC) stage, the virtual channel allocation (VA) stage, the Switch allocation (SA) stage, and the switch traversal (ST) stage. On the one hand, the complex router pipeline leads to aggressive speculation shorten the critical path through the router stages , the PS router still occupies a high ratio of communication latency when compared with one-cycle link delay in a mesh-connected NoC. On the other hand, the complex router pipeline leads to a high power ratio. In comparison with PS NoC, circuit switching can significantly lower the communication latency and power consumption, because routing and arbitration are not needed once circuits are set up. Only the ST stage is required on the circuit- switched (CS) connection when a flit traverses a node. However, circuit switching lacks flexibility. If several communications compete for a common physical channel, circuits will be set up in turn. Then, the long setup time will decrease the overall NoC performance. To address the problems of packet switching and circuit switching, the hybrid scheme [4]–[6] that combines packet switching and circuit switching is proposed. It not only can provide high flexibility for communications but also optimize latency of NoCs by establishing CS connections between communication pairs. It had been also demonstrated that establishing CS connections on the PS network can reduce communication power [6]. Moreover, before circuits have been established, packets are transmitted on PS connections to offset the long setup delay of circuits. However, the fact that CS connections are not allowed to share a common physical channel restricts the number of CS connections. If several packet transmissions will compete for a common physical channel, only one packet transmission can be executed in circuit switching and other packets must travel on PS connections. For the traffic with light congestion, most of communications can be addressed through circuit switching. However, for the traffic with heavy congestion, a very low ratio of CS connections to communications may be incurred, which limits the optimization of latency and power for NoCs. This paper focuses on further reducing the communication latency and power consumption of NoCs, because the communication latency of NoCs directly influences the data access latency in many-core systems, and the power

consumption of NoCs accounts for a high ratio of the total power consumption of the whole chip. In this paper, we propose a peculiar hybrid scheme, in which a novel switching mechanism, called virtual circuit switching, is first introduced to interweave with circuit switching and packet switching. In virtual circuit switching, virtual channels (VCs) are exploited to form a number of virtual CS (VCS) connections by storing the interconnect information in routers. Flits can directly traverse the router with only the ST stage. The main advantage of virtual circuit switching is that it can have the similar router pipeline with circuit switching, and can have multiple VCS connections to share a common physical channel. To support the proposed hybrid scheme, one modified router architecture is implemented based on the baseline with a tolerable overhead, and the corresponding switching mechanism is presented in this paper. Based on virtual circuit switching, a path allocation algorithm is proposed to determine VCS connections and CS connections on a mesh-connected NoC under a given network traffic, so that both communication latency and power consumption are optimized. A set of synthetic traffic workloads and real traffic workloads are exploited to evaluate the effectiveness of the proposed hybrid scheme. The experimental results show that our proposed hybrid scheme can efficiently reduce both the communication latency and power consumption. In summary, main contributions of this paper are listed as follows:

1) Virtual circuit switching is secondly introduced in this paper in new way, and the modified router architecture and its corresponding switching mechanism are presented to support the proposed hybrid scheme.

2) Based on virtual circuit switching, this paper uses a path allocation algorithm [13] to optimize both communication latency and power consumption.

3) The effectiveness of the proposed hybrid scheme is demonstrated by comparing with the baseline packed switched NoC and VIP design [6] using a set of synthetic and real traffic workloads.

The rest of this paper is organized as follows. Section II surveys some related work. Section III gives the presentation of the hybrid scheme based on virtual circuit switching.

II. RELATED WORK

Since the need for scalable on-chip communication architectures is pointed in [7] and [8], there are numerous literatures researching on optimizing latency or power consumption for NoCs. Some work focuses on designing customized communication architectures to reduce the global hop count using point-to-point connections or long range links [9]. Some work concentrates on evaluating different network topologies and developing a performance-and power-aware topology for NoCs. Some work considers developing algorithms for smartly mapping applications on NoCs, aiming at lower communication latency and power consumption. However, none of these literatures put forward to reducing the router-to-link latency/power for NoCs. Design methodologies for reducing the router-to-link latency/power on NoCs can be found in [4]–[6].

These methodologies can be classified into two categories. One category focuses on optimizing the microarchitecture of router. For example, the work in[4]–[6] preferred low power bufferless flow control for lightly loaded networks. However, bufferless flow control has a great effect on communication latency. The study in [13] proposed a 3.6-GHz single-cycle router for NoCs. A novel switch allocator was proposed to achieve high throughput and low latency. Kim [9] proposed a complete novel router microarchitecture, which could achieve simplicity, low latency, and low power simultaneously. One example can be the express VCs (EVCs). However, each EVC can only be established along one dimension. Connection is not limited by the dimension. More precisely, Stuart et al. [12] presented a reconfigurable circuit PS NoC for providing both power efficiency and flexibility. Jerger et al. [4] presented a hybrid NoC with on-demand circuit configuration. Abousamra et al. [5] developed the hybrid scheme in [4] to increase the utilization of circuits. A circuit setup and pining technique was proposed to keep the new circuit configuration stable until the end of a time interval. The network with virtual point-to-point (VIP) connections [6] is another hybrid circuit PS scheme for NoCs. A VIP is also a kind of CS connection. Different from the work in [4] and [5] that randomly set up CS connections, the hybrid scheme based on VIPs will trace the traffic pattern and set up as many low-latency low-power VIPs as possible through a smart algorithm. However, all these hybrid circuit PS schemes have a common problem that the restricted number of CS connections limits the optimization of latency and power consumption for NoCs. Different from the conventional hybrid circuit PS networks, this paper proposes a novel switching mechanism to address the problem of the conventional hybrid scheme mentioned above. In addition, further latency and power optimization for NoCs can be demonstrated, especially under the traffic with heavy congestion

III. PROPOSED HYBRID SCHEME BASED ON VIRTUAL CIRCUIT SWITCHIN

The basic principle of the proposed hybrid scheme is that VCs are exploited in virtual circuit switching to form a number of VCS connections and multiple VCS connections can share a common physical channel. In this hybrid scheme, VCS connections cooperate with PS

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connections and CSR outer Architecture In order to support VCS, PS,

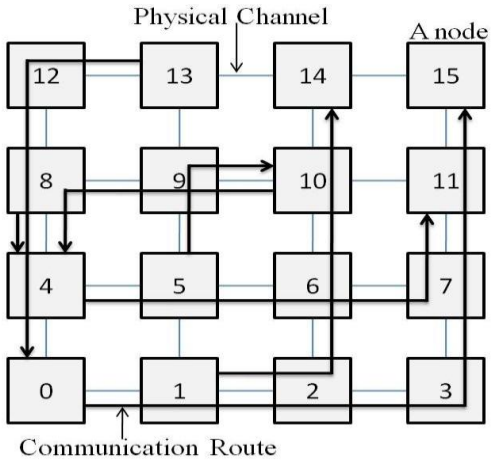

Fig.1 Simple traffic with communication routes in a 4 × 4 mesh.

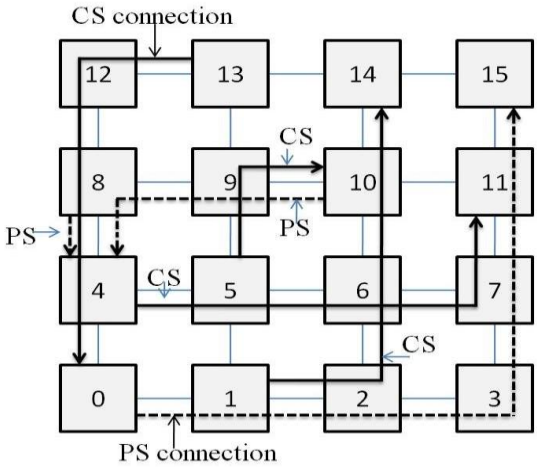

Fig.2. CS and PS connections of the conventional hybrid scheme.

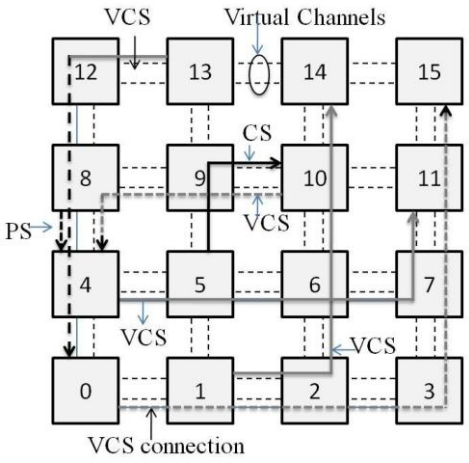

Fig.3. VCS, CS, and PS connections of the proposed hybrid scheme.

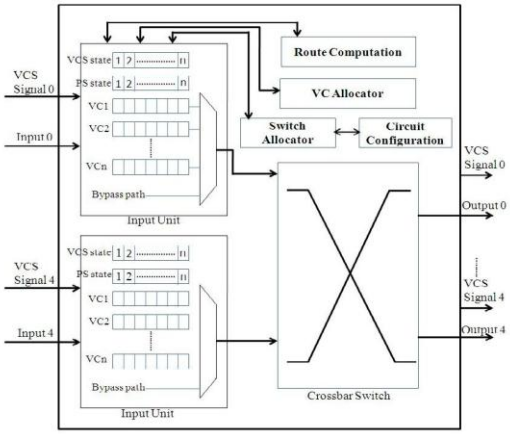

Fig. 4 Router Architecture

and CS connections at the same time, modified router architecture with five ports is proposed, as shown in Fig. 4. Compared with the baseline router [12], the additional hardware of the proposed router includes the bypass path, the circuit configuration, and the VCS state. First, the bypass path is added in each input unit for allowing flits to go directly to the crossbar switch. Second, each input unit contains a PS state and a VCS state. The PS state corresponds to the VC state of the baseline PS router, and the VCS state is used to support VCS connections. Third, the circuit configuration unit is to store the interconnect information for CS connections. In this paper, both the PS and the VCS states have n fields corresponding to n VCs. First, the VCS signal is only issued when crossbar switches of the VCS connection wait to be preconfigured. Due to the low activity of VCS signal, the power overhead caused by VCS signal can be much less than the power saving by bypassing buffer writing, routing, and arbitration of routers. Second, in the network with two VCs, th**e** width of VCS signal is 2 bits in Virtual Circuit Switching**.** The proposed hybrid scheme supports the interweaving of packet switching, circuit switching, and virtual circuit switching. Two extra bits are added to each flit to denote the switching type of the flit. When a flit enters the router, these extra bits are checked at first. Then, the corresponding router pipeline is executed according to the switching type of the flit. Operations of circuit switching in this paper are similar to [6]. This section mainly describes operations of virtual circuit switching. Note that VCS connections must be constructed in advance before the flit traveling in virtual circuit switching. Fig. 1 shows an example of traffic, in which physical channels (1, 2), (7, 11), and (8, 4) are shared by more than one communication, respectively. *(x, y)* denotes the physical channel from node *x* to node *y*. Fig. 2 shows CS connections and PS connections after using the conventional hybrid scheme. A CS connection is configured by recording in each router which input

port should be connected to which output port. It is composed of physical channels and routers.

However, routers on a PS connection are configured during the (BW, RC, VA, and SA) stages when flits require passing through. A physical channel can be shared by one CS connection and multiple PS connections. Once flits on CS connections arrive at routers, crossbar switches are immediately configured so that the CS flits can bypass directly to the ST stage [4]–[6]. When there is no CS flit, the corresponding ports of crossbar switches are released to PS connections. Fig. 3 shows VCS, CS, and PS connections of the proposed hybrid scheme. A VCS connection comprises VCs and routers that have been configured by recording in each router which input VC should be connected to which downstream VC. Crossbar switches of routers are preconfigured during the SA stage before VCS flits require passing through. Because VCS connections are established over VCs, a physical channel can be shared by *n* VCS connections at most (*n* is equal to the VC number). Other communications competing for that physical channel must be executed in packet switching, such as the communication from node 8 to node 4 in Fig. 3.

IV. SYNTHESIS RESULT

The proposed router and the baseline PS router are both implemented in VHDL. The fig. 5 shows the merging of circuit switching and packet switching. And the mixed flits are travelled on a single physical channel. This results in minimization of power and latency too. Fig. 6 shows that virtual circuit switching shares a common physical channel.

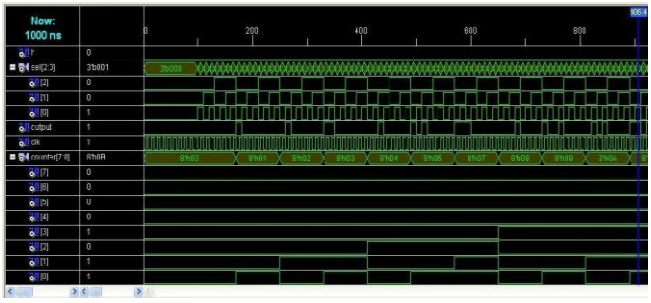

Fig. 5. Mixing of PS and CS

V. CONCLUSION

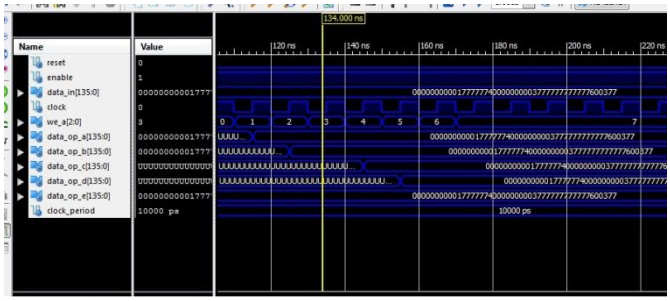

Fig .6 VCS sharing common physical channel

In this paper, we present an improved hybrid scheme based on virtual circuit switching to further reduce communication latency and power of NoCs. The basic principle of the proposed hybrid scheme is to mix virtual circuit switching with circuit switching and packet switching. Transitional router pipelines are bypassed by establishing VCS connections and CS connections. Our future work will focus on extending the current work to support applications with unpredictable communication patterns. Additional features of this paper include the fault tolerance, the quality of Service (QoS) operation, the multicast delivery service, and the mapping, scheduling of applications based on virtual circuit switching.

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