

HDL Design for Exa Hertz Clock Based $2e^{10}-1$ Exa Bits Per Second (Ebps) PRBS IP Core Generator for Ultra High Speed Wireless Communication Products

Prof. P. N. V. M Sastry¹
Dean- IT EDA Software¹
R&D-CELL & ECE Dept.
J.B.R.E.C., Moinabad, R.R
District.
Hyderabad-75 ,India
shastrypnvm@gmail.com

Prof. G. Krishnaiah²
ECE Dept., J.B.R.E.C
Moinabad, R. R. Dist.
Hyderabad-75 ,India
krishh786@gmail.com²

Prof. Dr. D. N. Rao³,
Principal²
J.B.R.E.C
Moinabad, R.R District.
Hyderabad-75 ,India
principal_jbr@yahoo.com³

Dr. S. Vathsal⁴
Dean- R&D& EEE²,
J.B.I.E.T
Moinabad, R.R District.
Hyderabad-75 ,India
svathsal@gmail.com⁴

Abstract: The Design is mainly Intended for High Speed Random Frequency Carrier Wave Generator of 1 Ebps Data Rate using $2e^{10}-1$ Tapped PRBS Pattern Sequence. The PRBS is Designed by using LFSR Linear Feed Back Shift Register & XOR Gate with Specific Tapping Points as per CCITT ITU Standards. RTL Design Architecture Implemented by using VHDL &/ Verilog HDL, Programming & Debugging Done by using Spartan III FPGA Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially / Parallel lines I/O.

Keywords: CCITT – Consulting Committee for International Telegraph & Telecom , ITU – International Telecom Unit, RTL- Register Transfer Level, LFSR-Linear Feedback Shift Register, VHDL- Very High Speed Integrated Circuit Hardware Description Language, PRBS-Pseudo Random Binary Sequence.

I. INTRODUCTION

In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga/Tera bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing , wireless Internet Data Packets Transceivers Computing, Tablets, Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers, NOCs, Network Cards/ Racks, WiFi, GiFi, Wimax, GPS, GSM, QCDMA Tranceivers.For that purpose , I Designed Exa Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for Hi-Fi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7, 10, 15, 23, 31 at a Clock carrier frequency speed of Exa Bits Per Second Ebps. The Length of PRBS sequence is 2^L-1 . 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM

Communication Systems, WiFi, GiFi, LTE, Wireless OFDMA , CDMA, QCDMA Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms (Exa Bits Per Second) Ebps . All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150, O.151, O.152 Standards. This PRBS Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Ebps Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & CRC.

XOR GATE

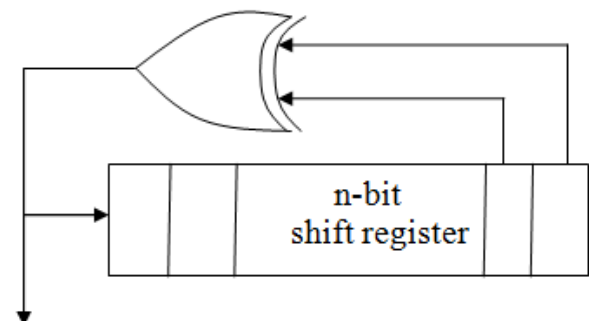


Figure 1.PRBS DESIGN-Fibonacci (many-to-one)Realization of LFSR with minimum number of taps and XOR gate in its feedback.

II. $2e^{10}$ -1 Exa Bits Per Second PRBS DESIGN ARCHITECTURE

Ebps Clock

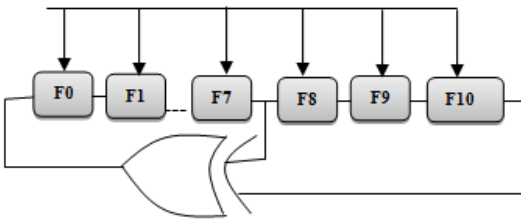


Figure 2. $2e^{10}$ -1 Ebps Rate PRBS Design

III. SOFTWARE – VLSI IC DESIGN FLOW

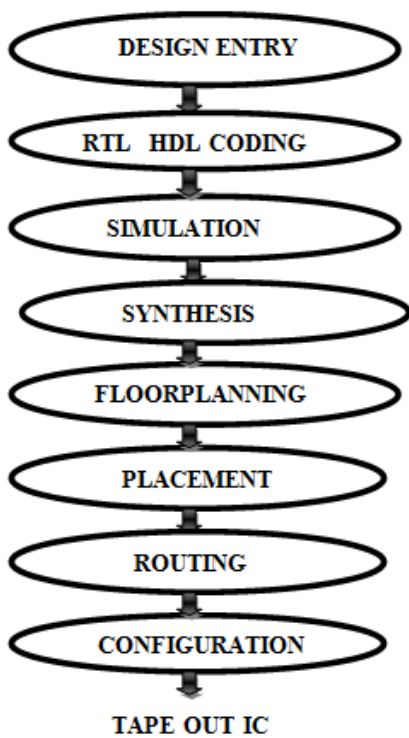


Figure 3. VLSI IC Design Flow Chart

IV. DESIGN FLOW REPORTS

A) $2e^{10}$ -1 Ebps Rate PRBS DESIGN RTL BLOCK

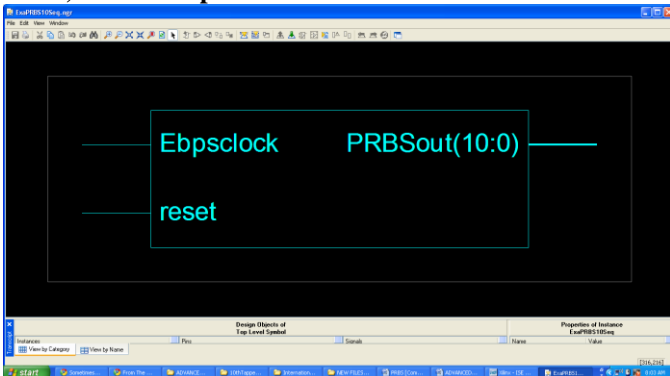
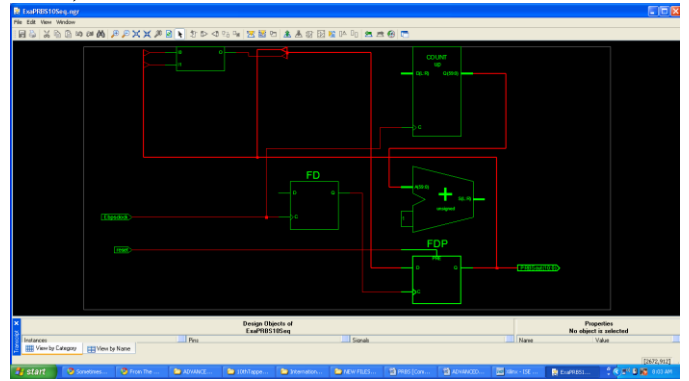


Figure 4. RTL Design Block $2e^{10}$ -1 Ebps PRBS\

B) RTL Schematic



C) FLOOR PLANNER DESIGN

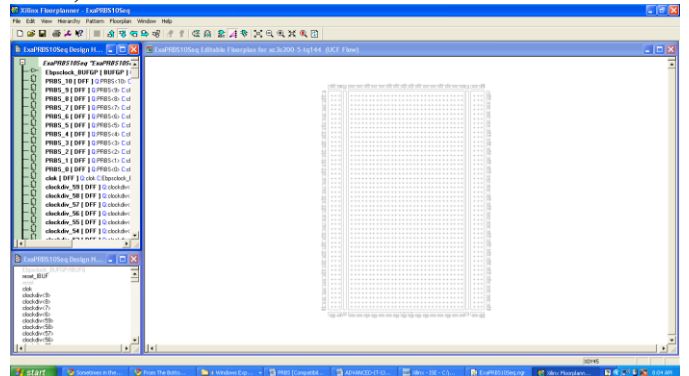


Figure 5. Floor planner Design $2e^{10}$ -1 Ebps PRBS

D) DESIGN PLACED REPORT –Ebps PRBS

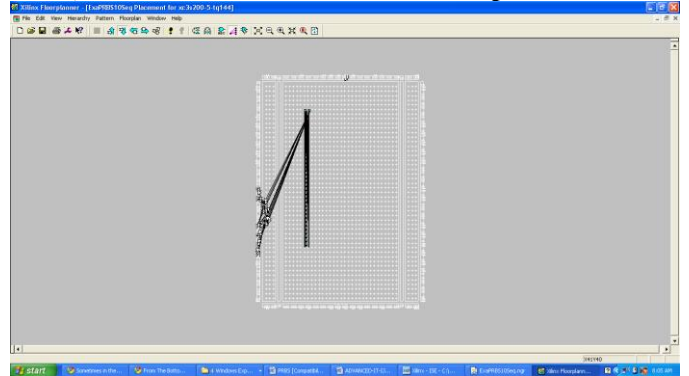


Figure 6. Placed Design $2e^{10}$ -1 Ebps PRBS

E) DESIGN ROUTED REPORT –Ebps PRBS

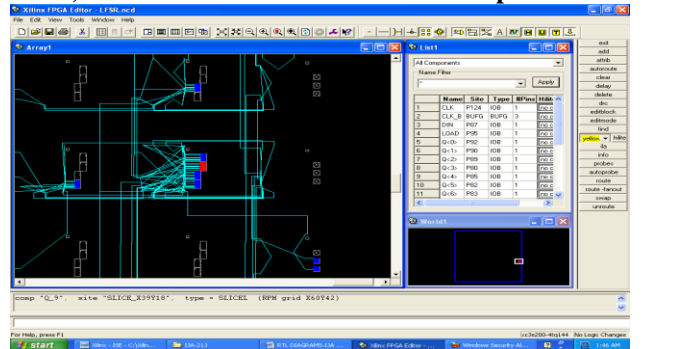


Figure 7. Routed Design Report $2e^{10}$ -1 Ebps

PRBS

F) SIMULATION WAVE FORM RESULTS

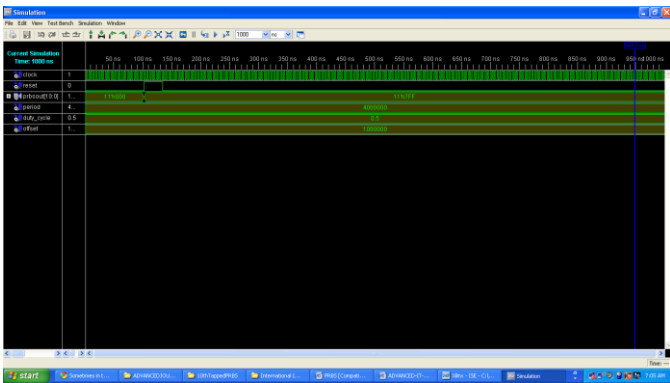


Figure 8. Simulation Results- $2e^{10}$ -1 Ebps PRBS

V. CONCLUSION

Designed High Speed Random Carrier Frequency Generator for Ultra High Speed Wireless Communication Engineering Products

VI. REFERENCES

- 1.http://en.wikipedia.org/wiki/Pseudorandom_binary_sequence
- 2.ITU – CCITT Reference Document

VII. Bibliography



Prof.P.N.V.MSastry Currently working with a Capacity of **Dean- IT EDA Software – R&D CELL & ECE DEPARTMENT**, He Did Master Degree In Science- M.S Electronics, Under Department Of Sciences, College Of Science & Technology AU -1998.Did PG Diploma In VLSI Design From V3 Logic Pvt Ltd B'lore-2001, Did M.Tech (ECE) From IASE Deemed University-2005. Currently Pursuing (PhD)-ECE(VLSI) , **JNTU Hyderabad -2012** , Over **Past 16 years of Rich Professional** Experience with Reputed IT Software Industrial MNC's, Corporate –**CYIENT (INFOTECH), ISiTECH** as a **world top keen IT Industrial Software Specialist – World Top Software Engineering Team Leader(Level 6) Eng-Eng- HCM Electronics Vertical & Program Manager – MFG I/C,EDS,BT,NON BT**

Embedded Software ,Avionics & Automotive Hi-tech Software Engineering Verticals & Departments , Program Lead – Embedded & VLSI & Engineering Delivery Manager – IT Semiconductor Software Engineering Vertical ,at ISiTECH , also worked with **Govt R&D, Industrial Organizations, Academic Institutions** of Comparative Designations & Rolls . His Areas Of Interest are VLSI –VHDL, Verilog HDL, ASIC, FPGA & Embedded Software Product Architectures Design & Coding Development .He mentored & Architecting Various Real Time, R&D ,Industrial Projects/Products related to VLSI & Embedded System Software & Hardware.. His Key Achievements are Participated Various Top Class International IT MNC Delegates Board Meetings, IT Software MNC Board Meetings(Tier1/2 Level MRM-VP,COO Level) , Guided R&D ,Industrial , Academic Projects /Products –VLSI-ASIC,FPGA & Embedded & Embedded,VLSI Software Project &/ Program Management & Also Coordinated Various In House & External IT Project Workshops & Trainings At **CYIENT(INFOTECH)** as a I/C- MFG Eng Software Vertical , Also Participated Various National R&D Workshops, FESTS, FDP's & Seminars. Recently He Published Various national & International Journals



G.Krishnaiah, Pursuing Ph.D from JNTU UNIVERSITY,Hyderabad, India. Currently working as a Professor, in the Department of Electronics and communication Engineering, Joginpally B.R Engineering college, Hyderabad, Telangana State, India. His carrier spans nearly 19 years in the field of teaching, administration, R&D, and Industry & Research. He has actively involved in organizing various conferences and work-shops. He has published over 4 international journal papers out of his research work. He presented more than 3 Research papers at various national and International conferences. He is currently a Life Member of ISTE, IETE,CSI, and Member of IEEE and MIE. He is also guiding the projects of U.G / P.G. students of various universities. His area of Research includes Digital Signal Processing; Image & Video signal Processing, Low power VLSI Design, Embedded systems, Wireless communication, Global Positioning systems and Pseudolite Systems.



Dr. D.N Rao B.Tech,M.E,Ph.D, principal of JBREC, Hyderabad. His carrier spans nearly three decades in the field of teaching, administration,R&D, and other diversified in-depth experience in academics and administration. He has actively involved in organizing various conferences and workshops. He has published over 11 international journal papers out of his research work. He presented more than 15 research papers at various national and international conferences. He is Currently approved reviewer of IASTED International journals and conferences from the year 2006. He is also guiding the projects of PG/Ph.D students of various universities



Dr.Srinivasan Vathsal Obtained **B.Tech-EEE** in 1968 from Madras University. He got **M.E** in EEE

from BITS Pilani in 1970. He Obtained **Ph.D.** from **School Of Automation, I.I.S.C, and Bangalore** in 1974. He Did **Two Year Post Doctoral Research** in DFVLR, Germany & **NASA Goddard Space Flight Centre, USA**. Under **NRC NASA** research fellowship for another two years .He has closely worked with **Dr.A.P.J Abdul Kalam in Project SLV of Vikram Sarabhai Space Centre** for four years in the mission analysis group.. On return from USA he worked in **DRDL, Hyderabad** as **Scientist E, F & G.** also Head of Non Destructive Evaluation Division, and officer In-Charge-Joint Advanced Technology Program, Indian Institute of Science. He also worked with Various Academic Institutions as a Professor, Dean of Science & Humanities & Director Energy Center for One Year. He has worked as Principal of Bhaskar Engineering College, Hyderabad for 2-years. Currently he is **Professor & Dean (R&D)-JBIET, Hyderabad.**

He has published 80 Technical papers in national & international journals & conferences. He is chief Editor of international journal Intelligent Automation (IJIA), from Korea.. He is Chief Editor of JBIET Research Review which is JBIET quarterly Journal. He is life senior member of IEEE .He is fellow IETE and Aeronautical society of India. He is also life member of System society on India, Instrument society of India and Astronautically Society of India.

Recently he delivered Invited lecture in University of Minnesota, Minneapolis USA.on Application of Kalman filtering for Power Electronics and Power systems.. He has guided 5 Ph.D students and currently guiding 8 Ph.D students.