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A Review on Implementation of Image Processing Algorithms using Hardware Software Co-simulation

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Abstract: Edge detection is necessary tool for extraction of information for further image processing operation. Many computer vision application use edge detectors as primary operators before high level image processing. Several algorithms are available for edge detection which makes use of derivative approach. Roberts, Prewitt , sobel, canny are some of the examples of edge detection methods. In this project edge detection algorithms are to be implemented over FPGA board. Proposed architecture gives an alternative by using a graphical user interface which is developed by combining MATLAB, Simulink and XSG tool. Prototype of Application Specific Integrated Circuit [ASIC] can be obtained by FPGA based implementation of edge detection algorithm. Comparative analysis using software and hardware is to be done. Instead of using traditional approach of programming FPGA, Xilinx System Generator [XSG] is used for programming and modeling FPGA. XSG has an integrated design flow to move directly to the bit stream file from simulink design environment which is necessary for programming the FPGA. Advantage of using FPGA is power efficient circuits can be fabricated; it has large memory and superior parallel computing capacity. With use of FPGA, design procedure becomes more flexible.

Keywords— *ASIC, FPGA,MATLAB ,Prewitt, Sobel, XSG.*

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I. INTRODUCTION

Edge detection is an essential preprocessing step in image processing. Edge detection is a set of mathematical rules with identifies the point in a digital image where the brightness of image sharply changes or has discontinuities. The need to find the sharp changes in an image is to capture all the significant event and property changes. In many applications it is necessary to find boundaries of objects that appear in images. Edge detection is always one of the classical studying projects of computer vision and image processing field. It is the first step of image analysis and understanding. The purpose of edge detection is to discover the information about the shapes and the reflectance or transmittance in an image. The correctness and reliability of its results affect directly the comprehension machine system made for objective world. Low level image processing operations like image segmentation using edge detection and feature extraction helps us to analyze, infer and take decision in various applications. It focuses on processing an image pixel by pixel and over its neighborhood. Image processing operations can be applied to the whole image or its parts.

The edge is characterized by its length, slope angle, and coordinate of the slope midpoint. Among several ways for performing edge detection; the majority may be grouped into two categories, Gradient and Laplacian based approach. The basic Edge detection operator is a matrix area gradient operator that determines the level of variance between different pixels. It is calculated by forming a matrix centered on a pixel chosen as the centre of the matrix area. If the value of the matrix area is above 2 a given threshold, then the middle pixel is classified as an edge. Examples of gradient based edge detectors are Roberts, Prewitt and Sobel operators. All the gradient based algorithms have Kernel operators that calculate the strength of the slope in directions that are orthogonal to each other, generally horizontal and vertical Clasically, Edge detection algorithms have been implemented over software plat-form. With advancement in the VLSI technology hardware implementation has become an attractive alternative. Assigning complex computation tasks to hardware and exploiting the parallelism and pipelining features yield significant speedup in running times. Implementation of image processing on re-configurable hardware, enables rapid prototyping of complex algorithm and simplifies debugging and verification. In recent years FPGAs (Field Programmable Gate Array) have become superior platform, with high-speed parallel computing capacity. FPGA is a fine grained device with large number of Input Output Blocks (IOBs) and Configurable Logic Block (CLBs) and other logic elements. FPGA is rich source of high speed multipliers, adder, and memory; in the design process they can be directly called. Subsequently it is easy to implement

complex convolution over this platform. FPGA based design offers an advantage of short Turn Around Time (TAT) and small Non Recurrent Expense (NRE). While implementing an algorithm over hardware platform, in the traditional approach, user needs to emulate the floating point algorithm in HDL code. Further, it can be tested and verified by repeated functional simulations, post simulation processes and finally generate bit stream file. Xilinx introduces the system modeling tool Xilinx System Generator.

RELATED WORK

EDGE DETECTION

Edge detection is one of the most commonly used operations in image analysis, and there are probably more algorithms in literature for enhancing and detecting edges. An edge is point of sharp change in an image, a region where pixel locations have abrupt luminance change i.e. a discontinuity in gray level values. In other words, an edge is the boundary between an object and the background. The shape of edges in images depends on many parameters like the depth discontinuity, surface orientation discontinuity, reflectance discontinuity, illumination discontinuity, and noise level in the images.

The main steps in edge detection are:

1. Filtering: It is gradient computation based on intensity values of two points which are susceptible to noise. Filtering reduces noise but there is a trade-off between edge strength and noise reduction.
2. Enhancement: It is done in order to facilitate the detection of edges, it is essential to determine intensity changes in the neighborhood of a pixel in an improved manner. Enhancement emphasizes pixels where there is a significant change in local intensity values and is usually performed by computing the gradient magnitude
3. Detection: It is done because many points in an image have a nonzero value for the gradient, but not all these points can be considered to be edges. Therefore, some method should be used to determine which points are edge points. Frequently, threshold provides the criterion for detection.

1. Prewitts edge detection algorithm: The Prewitt operator is based on the idea of central difference and is much better than Roberts's operator. It is based on convolving the image with a small, separable, and integer valued filter in horizontal and vertical direction as shown in equation. Prewitt's operator has longer support and is less vulnerable to noise.
2. Sobel edge detection algorithm: In sobel algorithm higher weights are assigned to the pixels close to the candidate pixel. The Sobel operator is first order edge detection operator, it computes gradient of the image as intensity function. The Sobel operator only considers the two orientations which are 0 and 90 degrees as convolution kernels. Absolute magnitude of the gradient at each point of image can be obtained by merging Kernels together.
3. Canny edge detection algorithm: The 3 phases in Canny edge detection algorithm are (1) smoothing and differentitation: The input image is smoothened with a Gaussian and the gradient is obtained in the x and y directions.(2)Non maximal suppression :This phase is used to eliminate edges that are not maxima in the direction perpendicular to the edge. (3) Thresholding: It is used to eliminate edges lower than threshold T1, keeping edges greater than threshold T2.

II. LITERATURE REVIEW

An extensive work is done in the field of edge detection for real time image processing. In recent years, in September 2009[8] the algorithm implementation for FPGA based design for various applications using edge detection was proposed. The hardware processing on an FPGA allows the capture and online processing in real time on the same chip. External memory module can be saved using memory from FPGA only. The rate achieved by PC is greater than FPGA because PC clock is much higher than FPGA. In another paper [7] improvement was done by using block RAM and IO interface on the FPGA. After this in 2010 the improvement [6] was done by implementing the hardware circuit of the algorithm on ISE 9.1 and simulated in Model sim 6.0.It gave high precision edge. When the system is validated, it indicates that the video image edge detection system can detect high precision edge. This paper realises a hardware based video edge detection system on FPGA mainly by the completion of the system IP core. Next stage was achieved by using A Moving Window Architecture in MAY 2012[5] which performs the more computational complex operations of edge detection algorithm like non maximum suppression and double thresholding By using this design results are stored within the FPGA and eliminates the needs of large memory buffer. Improvement over this was done using FPGA Accelerated object detection using edge information. This paper proposes an FPGA based object detection that utilises edge information to reduces the search space involved in object detection. This indicate

performance speed up and energy saving rating compared to traditional Moving Window approach.The proposed architecture in this paper [4] are providing a platform for real time alforithm on application specific hardwre with higher performance than programmable digital signal processors. In 2011 edge detection algorithm [3] for prewitt and sobel was presented and compared their result. After that A methodology [2] for real time architecture for Edge detection using sobel filter for image processing using Xilinx System Generator. In this approach a Virtex 5 FPGA kit is used to achieve higher performance than previous methods. In 2013 Paulo possa presented [1]a new flexible architecture for image and video processing with reduced latency and memory requirements supporting a variable input resolution. The proposed architecture is optimized for feature extraction such as the canny edge detector and the Harris corner detector. Also algorithm simplications are employed to reduce mathematical implementations on an FPGA based modules. It has clear advantage in low level power applications, low latency and portability are required.

III. PROPOSED WORK

- The objective of our project is to implement various edge detection algorithms using FPGA kit.

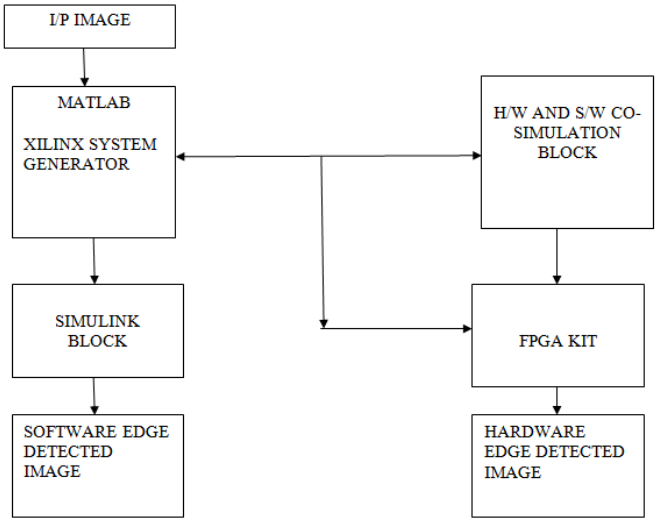
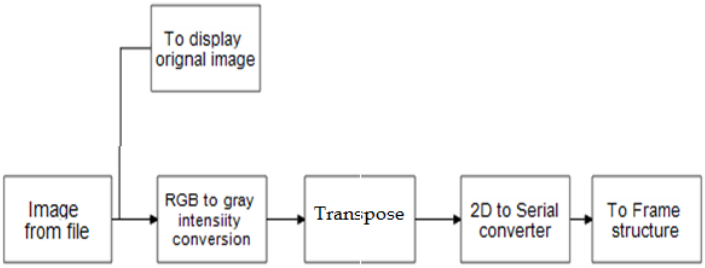


Fig-1: Block Diagram

Software implementation:

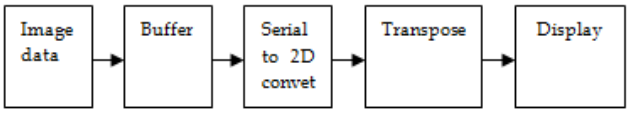
1. Initially the original digital image which may be color is first converted into Grey scale image using MATLAB.
2. This 2-D image is then converted into 1-D for further processing. This 1-D data stream is given to Frame conversion block.
3. At this point edge detection using XSG is done. This is followed by arithmetic blocks to merge all processed data.
4. The 1-D output of XSG block set are given to image post processing blocks to obtain original 2-D image with its edge detected.

For the design of filters to meet hardware requirements, it is a must to pre-process the image prior to the main hardware architecture. In the software level simulation using Simulink block sets alone, where the image is used as a two-dimensional(2D) arrangement such as M x N, there is no need for any image pre-processing, but at hardware level this matrix must be an array of one dimension(1D), namely a vector, where it requires image pre-processing. Image Pre-processing Block sets



The model based design used for image pre-processing is shown. The blocks utilized here are discussed below. Input images which could be color or grayscale are provided as input to the File block. A color space conversion block converts RGB to grayscale image and this data which is in 2D is to be converted to 1D for further processing. Frame conversion block sets output signal to frame based data and provided to unbuffer block which converts this frame to scalar samples output at a higher sampling rate.

The image post-processing blocks which are used to convert the image output back to floating point type.



For post-processing it uses a Buffer block which converts scalar samples to frame output at lower sampling rate, followed by a 1D to 2D (matrix) format signal block, finally a sink is used to display the output image back in the monitor, utilizing the Simulink block sets.

IV. CONCLUSION

Real time applications are always on hardware platform rather than software. In this paper low level digital image processing technique which is edge detection algorithm over software and hardware platform is proposed. Several edge detection algorithms are available But we are implementing them on hardware platform using Xilinx system generator tool. XSG tool of MATLAB provides simpler and efficient way of FPGA programming.

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