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Design of Wallace Tree Multiplier with Power Efficient Adiabatic Logic

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***Abstract*—**The objective of this project is to design high performance arithmetic circuits which are faster and have lower power consumption using a new adiabatic logic family of CMOS and to analyze its performance for sequential circuits and effects upon cascading. It commencement on evaluation of a computational block before its evaluation phase begins, and quickly performs a final evaluation as soon as the inputs are valid. This adiabatic logic family is best suited to arithmetic circuits because the critical path is made of a long chain of cascaded inverting gates.In this paper we are going to design Wallace Tree Multiplier using full adder structure with adiabatic logic. As the major advantage of this logic which is higher speed and low power consumption is observed upon cascading, it is most suitable for arithmetic circuits.

Keywords*—Adiabatic logic; Low power VLSI circuit; Arithmeic Circuits.*

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I.INTRODUCTION

Digital electronic computations began with the introduction of vacuum tubes. In the era of vacuum tube based computer, machines like ENIAC and UNIVAC were developed. It was consist of 18,000 vacuum tubes and was 80 feet long with several feet of height and width. This clearly tells about the low integration density problem of vacuum tubes. So implementation of larger engines became economically and practically infeasible. The invention of the *transistor*, followed by the introduction of the bipolar transistor led to the first successful IC logic family, *TTL (Transistor-Transistor Logic)*.

TTL had the advantage, of a higher integration density and on this; the first integrated circuit revolution was based. Ultimately, the large power consumption per gate put a restriction on the number of devices that can be reliably integrated on a single chip.

Next was the turn of the MOS digital integrated circuit approach. Initially MOS ICs were implemented in PMOS only.As electrons have higher mobility than holes, NMOS was preferred later.

The second age of the digital integrated circuit revolution began with the introduction of microprocessors by Intel (4004) and 1974 (8080). These processors used NMOS-only logic, with higher speed relative to the PMOS logic. But later, NMOS-only logic started suffering from the same problem: power consumption. Finally the balance tilted towards the CMOS technology, where we are still today. Power consumption concerns are again becoming dominant in CMOS design as well. Unfortunately, this time there does not seem to be a new technology coming up any time soon. So what we can do is make slight modifications in the logic style so as to improve speed and reduce power consumption.

In case of CMOS, addition of a single input increases the device count by 2 and thus increases the propagation delay. New logic styles were developed to minimize the propagation delay and chip area. So forms of CMOS circuits are searched to supplement the static CMOS logic that can be used in specific applications. Then Dynamic logic came into picture which works as per clock. It has higher speed as well as lower power but suffers from cascading problem which led to Domino and NORA logic styles.

A.Wallace Tree Multiplie

A **Wallace tree** is an efficienthardware implementation of a digital circuit that multiplies two integers, was invented by an Australian Computer Scientist Chris Wallace in 1964. The Wallace tree has three steps:

1. Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, yielding n^2results. Depending on position of the multiplied bits, the wires carry different weights, for example wire of bit carrying result of a_2b_3 is 32 (see explanation of weights below).
2. Reduce the number of partial products to two by layers of full and half adders.
3. Group the wires in two numbers, and add them with a conventional adder.

The second phase works as follows. As long as there are three or more wires with the same weight add a following layer:

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- Take any three wires with the equal weights and input them into a full adder. The result will be an output wire of the same weight and an output wire with a higher weight for each three input wires.
- If there are two wires of the same weight left, input them into a half adder.
- If there is just one wire left, connect it to the next layer.
- THE well-known Wallace high-speed multiplier uses carry save adders to reduce an N-row bit product matrix to an equivalent tworow matrix that is then summed with a carry propagating adder togive the product [1].

Wallace high-speed multipliers use full adders and half adders in their reduction phase. Only the use of half adders don't reduce the number of partial product bits. Therefore, to reduce the complexity,it is beneficial to minimize the number of half adders used in a multiplier reduction. An advancement to the Wallace reduction is presented that ensures that the delay is the same as for the conventional Wallace reduction. The modified reduction method greatly reduces the number of half adders; producing implementations with 80 percent fewer half adders than standard Wallace multipliers, with a very slight increase in the number of full adders[2].Very few researchers havereported work on approximate multipliers. Sullivan et al. used$TruncatedErrorCorrection$(TEC) to investigate an iterative approximate multiplier in which some amount of error correcting circuitry is added for each iteration.Thisanalysis indicates that this design gives up to a 50% efficiency advantage relative to prior flexible approximate multipliers study proposed a flexible approximate multiplier with improved efficiency.[3] A new power and area efficient approximate Wallace multiplier is designed in the paper[4] which provides high accuracy.Authors mainly focussed on the accuracy and they achieve more than 90% accuracy.There is a scope in reduction of power.

B.ADIABATIC LOGIC

The power consumption of the electronic devices can be reduced by adopting different design styles. Adiabatic logic style is said to be an attractive solution for such low power electronic applications. This paper [6] gives anidea of energy efficient technique for digital circuits that uses adiabatic logic.Adiabatic logic is commonly used to reduce the energy loss during the charging and discharging process of circuit operation. Adiabatic logic is also known as "energy recovery" or "charge recovery" logic. As the name itself indicates that instead of dissipating the stored energy during charging process at the output node towards ground it recycles the energy back to the power supply thereby reducing the overall power dissipation and hence the power consumption also decreases. The adiabatic logic uses AC power supply instead of constant DC supply, this is one of the main reasons in the reduction of power dissipation.The adiabatic logic can be explained with the help of basic inverter circuit[6].

Adiabatic logic can be explained with the help of following example of inverter circuit.

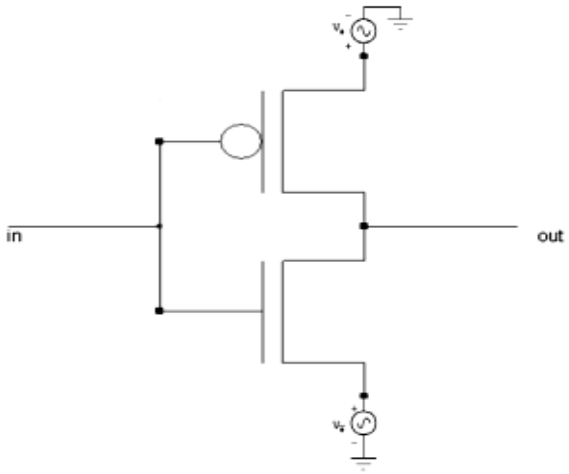

Fig.1(a)Adiabatic inverter

The adiabatic inverter circuit can be constructed using CMOS inverter with two AC power supplies instead of DC supply. The power supplies are arranged in such a way that one of the clock is in phase whereas the other is out of phase with the first one. The operation of the adiabatic inverter can be explained in two stages. During the charging phase, the PMOS transistor conducts and NMOS transistor goes into OFF state which charges the output load capacitor towards the power supply results in logic HIGH output.

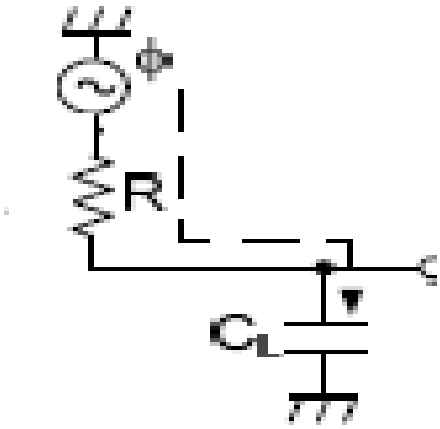

Fig .1 (b) Equivalent circuit for charging process in adiabatic inverter

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	Logic style	Power dissipation (Watts)	Memory Space allocated(bytes)	Average no. of Newton iterations	Number of transistors	Latency (%)
DIFFERENCE	CMOS	3.1377E-10	43274240	4.127500	28	0.0000
	ECRL	4.2591E-07	43274240	4.865462	28	0.0000
	PFAL	1.2857E-10	43274240	4.671111	30	0.0000
	2PASCL	1.0448E-11	43274240	4.384416	28	0.0000
	PFAL&2PASL	3.7782E-11	43266048	4.371084	32	0.0000
BORROW	CMOS	1.9911E-10	43282432	3.638146	18	0.0000
	ECRL	6.5905E-07	43282432	4.655311	18	0.0000
	PFAL	1.3461E-06	43286528	4.225806	20	0.0000
	2PASCL	9.1542E-12	43282432	4.307487	18	0.0000
	PFAL&2PASL	2.8266E-11	43286528	3.988473	22	0.0000

Table 1.Comparison Of Different Parameters of Full Subtractor in Adiabatic logic with CMOS

Table shows that the power dissipation of different adiabatic logic styles is lesser than the conventional CMOS design. The power supply that is given to the adiabatic circuits is also lesser than the conventional CMOS design.[6].

PROPOSED WORK

In our project our approach is to design a full adder circuit with adiabatic logic which is previously designed using a CMOS logic [5]. And design our Wallace multiplier using these adiabatic full adders.

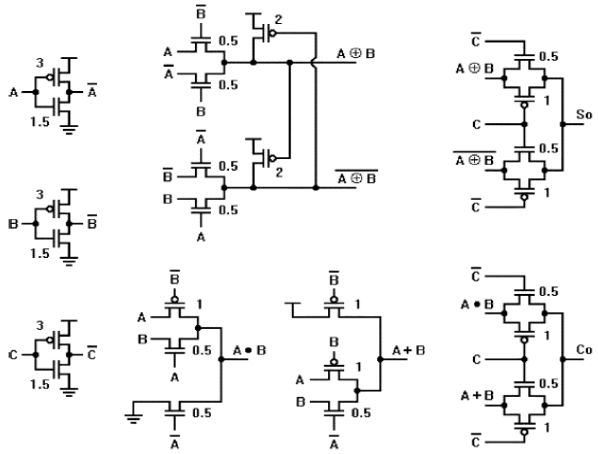

Fig.2.Proposed Full Adder Cell With AdiabaticLogic Style

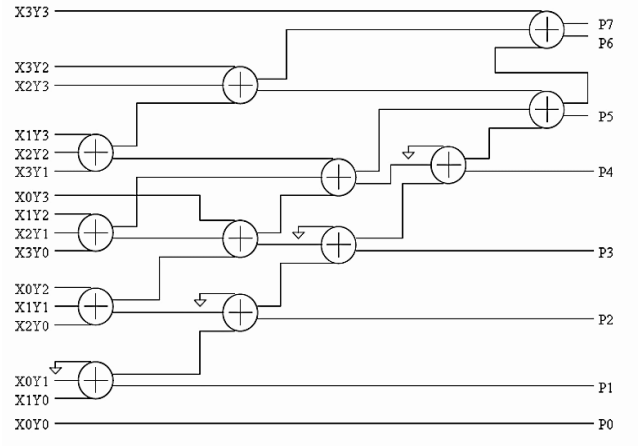

Fig.3. Proposed Wallace Tree Multiplier

In This Paper We Are Concentrating On The Designing Of Wallace Tree Multiplier By Using CMOS Power Efficient Fulladders To Reduce No Of Gates Using Adiabatic Logic Architecture.With A Use Of Sub Deep Micron Technology.

An Alternative Internal Logic Structure For Designing Full Adder Cells Was Introduced[5].In Order To Demonstrate The Advantages Two Full Adders Were Built In Combination With Pass Transistor Powerless Groundless Logic Style.

We Are Going To Design This Full Adder With Adiabatic Logic And We Will Compare The Conventional CMOS Full Adders With Adiabatic Full Adder Structure In Terms Of Power Dissipation.

Our Main Aim Is To Design A Wallace Tree Multiplier With These Adiabatic Logic Full Adder Structures.

CONCLUSION

From Previous Work Related To Designing Of The Wallace Tree Multiplier With A CMOS Technology, There Is Ascope Of Power Reduction, Increase In The Cascaded Stage,The Delay Automatically Increase So There Is Scope To Reduce The Delay By Working On Cascaded Stages.

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