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Comparative Analysis of Grid side Converters for Leakage Current Reduction

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***Abstract*—** Design of grid side converters comprises of galvanic isolation between the grid and DC supply .Now a days, for low power applications are effecting more because of high leakage current due to parasitic effect between grid and DC supply, in order to limit the ground leakage current (which deteriorates the power quality and generates EMI), new converter topologies have been proposed. This paper proposes the comparative analysis of H5 and H6 topologies in the aspects of leakage current reduction, parasitic capacitance effect and voltage balancing across the dc mains. The performances of the topologies are also analyzed by implementing modulation techniques. Simulated and tabulated results of H5 and H6 topologies conclude the performance evaluation.

Keywords- *DC-AC power conversion; multilevel systems; Pulse width modulated inverter; Pulse width modulation*

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I. INTRODUCTION

The power converter is a topology that enables the efficient and flexible interconnection of different players (which are renewable energy generation, energy storage, flexible transmission and controllable loads) to the electric power system. Hence renewable energy sources will be a major player in the future of power system based on smart grid technologies [1]. Recently, converter topologies are employing high frequency transformer in order to reduce size and weight. The trade of between high efficiency and low cost is a hard task for these kind of architectures because their several power stages. In low power applications, as per international standards, the grid connected power converters allows the transformer less architectures without any galvanic isolation[2].

In PV-grid side converters, the ground leakage current must be less than one ampere, but it is very difficult to get minimum ground leakage current in transformer less system [3]. The schematic diagram is depicted in Fig.1, which represents the use of modulation techniques with pulse generator block. Converter can be either H5 or H6 topology with grid parameters as shown. However comparison made between H5&H6 topologies are in the aspect of ground leakage current and parasitic effect.

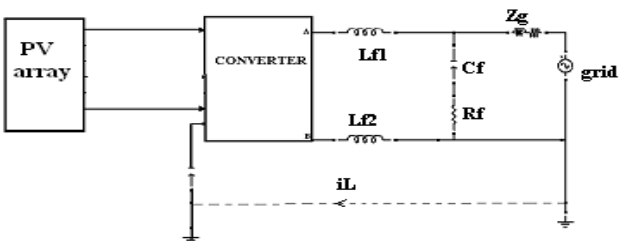

Fig.1. Path of the common mode current in transformer-less system

This paper is discussed about modes operation of H5 and H6 topologies in section II. Section III details about grid connected multi level inverter topologies. Section IV briefly details the comparative analysis between two topologies in the presence of PV grid system. Section V discussed closed loop operation of efficient topology. Section VI reports simulation results about the numerical values tabulated regarding the performance parameters and Section VII concludes the objectives of the paper and discusses about future scope.

II. THE CONFIGURATION OF SINGLE PHASE FIVE LEVEL TOPOLOGIES

Multilevel converters are nowadays widely adopted; the basic idea is that the dc-link voltage can be split between different capacitors, which can provide intermediate voltage levels between the reference potential and the dc-link voltage. The configurations of the H5 and H6 topologies are described in the following.

A. H5 topology:

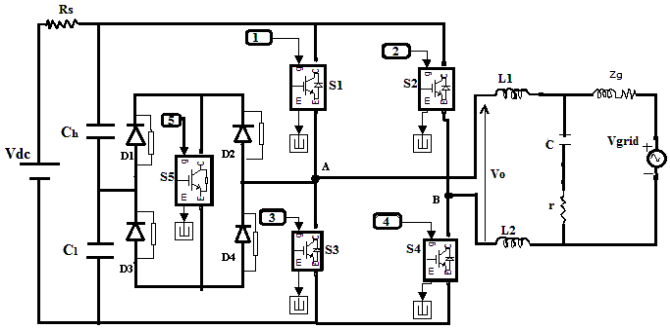

Fig.2. Architecture of the H5 topology in [2]

The H5 converter is constituted by a full-bridge with an additional bidirectional switch (realized with an IGBT and four diodes), employed to connect the midpoint of the dc link to the converter output. With reference to the schematic in Fig. 2, the operation of the H5 for five-levels in output are as shown in Fig. 2 with the configuration of switching pulses tabulated in table1.

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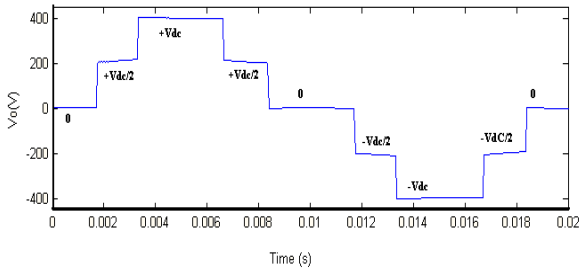

Fig.3. generalized single phase multi level inverter output voltage

TABLE I. SWITCHIN STATES OF H5 TOPOLOGY

VOLTAGE LEVEL	S1	S2	S3	S4	S5
V_{dc}	1	0	0	1	0
$V_{dc}/2$	0	0	0	1	1
0	0	0	1	1	0
$-V_{dc}/2$	0	1	0	0	1
V_{dc}	0	1	1	0	0

From Table1, it can be noticed that every level of output voltage is synthesized with the help of two switches. All switches used in the H5 topology are IGBT's. Three of them could operate at switching frequency are S1, S3, S5 and remaining two switches S2 and S4 operated at line frequency. The output of H5 topology consists of large contribution of harmonics; hence it is needed filter components to attenuate the higher order harmonics before feeding grid.

B. H6 topology:

This topology has six switches in its architecture to obtain multi level inverter output. Among six switches, four switches are IGBTs and remain two switches are MOSFETs. Moreover MOSFETs (S5 and S6) are operated at switching frequency and remain four IGBTs are at line frequency. On state resistance of the MOSFETs is low compare with IGBTs so that the overall conduction losses of the inverter are comes down than H5 topology. To obtain output level of V_{dc} four switches being conducting where as in H5 topology only two switches were ON. This implies H6 topology has low voltage stresses than H5 topology.

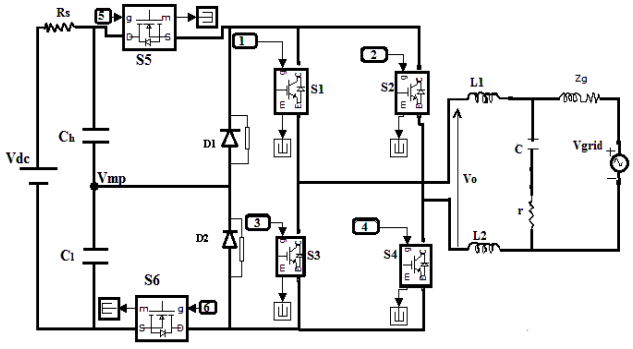

Fig.4. Architecture of the H6 topology

Working operation of H6 topology is explained with the help of Table2 which represents the switching configurations. It can be observed that for the voltage level V_{dc} can be synthesized with the help of four switches, $V_{dc}/2$ with the help of three switches and zero voltage level can be achieved by two switches only [4].

TABLE II. SWITCHIN STATES OF H6 TOPOLOGY

VOLTAGE LEVEL	S1	S2	S3	S4	S5	S6
V_{dc}	1	0	0	1	1	1
$V_{dc}/2$	1	0	0	1	0	1
0	1	1	0	0	0	0
$-V_{dc}/2$	0	1	1	0	1	0
V_{dc}	0	1	1	0	1	1

III. GRID CONNECTED TOPOLOGIES

The quality of generated energy is crucial, when it is fed to the grid, the non sinusoidal output causes additional voltage drop across the line impedances. This leads to voltage distortions at grid side. The circuit calls filter for reducing distortions and getting pure sinusoidal shape. So that filter must be design precisely. The size and cost of the filter comes down whenever output voltage levels of inverter are improved.

The own design of the filter is a compromise between the values of the capacitance and inductance. Inductor attenuates high-frequency signals and allows low-frequency signals, while capacitors do the reverse. A filter in which the signal passes through an inductor, or in which a capacitor provides a path to ground, presents less attenuation to low-frequency signals than high-frequency signals and is therefore a low pass filter. Resistors on their own have no frequency-selective properties, but are added to inductors and capacitors to determine the *time-constants* of the circuit, and therefore the frequencies to which it responds.

The transfer function of the grid connected multi level inverter topologies is as shown in equation (1)

$$H(j\omega) = V_g(j\omega)/V_o(j\omega) \qquad (1)$$

Second order filter has better damping behavior than L-filter. The overall grid parameters which are used in this paper are shown in table3.

TABLE III. SINGLE PHASE GRID PARAMETERS

PARAMETER	VALUE
Inductor (L_{f1}=L_{f2})	1mH
Capacitor (C_f)	2μF
Damping resistor (R_f)	0.5Ω
Grid impedance (Z_g)	Jw50μH+0.4Ω

The designed filer is attached at the output terminals of either H5 or H6 topologies. These two inverters are simulated with a switching frequency of 15 KHz with the dc supply of 380V and modulation index of 0.87.the tabulated values of table4 are the evidence of declaring the effectiveness of filter.

TABLE IV. EFFECTIVENESS OF THE FILTER

	Before filter [V_o]		After filter [V_g]	
Topology	***Fundamental***	***%THD***	***Fundamental***	***%THD***
H_5	334.2v	32.86	327.2v	0.95
H_6	331.8v	34.70	328.8v	1.10

IV. PV-GRID CONNECTED CONVERTERS

PV system is one of the clean technologies for producing electricity. The PV module has designed in the matlab/simulink with the aid of mathematical equations. The designed module is in-charge for short circuit current of 3.807A, open circuit voltage of 1000V, and series resistance of 0.1147Ω. Fig.5 presents architecture diagram of PV-grid connected systems. This remains as the input same for both H5 and H6 topologies.

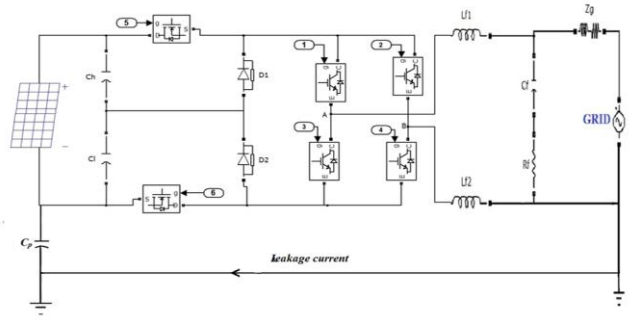

Fig.5.Schematic diagram of PV-grid connected H6 topology

The PV module served for 380V as input voltage of the converter during conduction. Parasitic capacitance between the output and the input can act as a feedback path, causing unwanted oscillations and it is deteriorates the system with enhancing leakage current. At low frequencies parasitic capacitance can usually be ignored, but in high frequency circuits it can be a major problem.

The performance of H5 topology as well as H6 topology is also deteriorates with the parasitic effect. Those results are self explanation in fig.6.

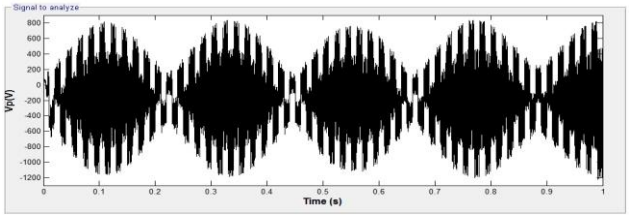

Fig.6 (a).H5 topology parasitic voltage

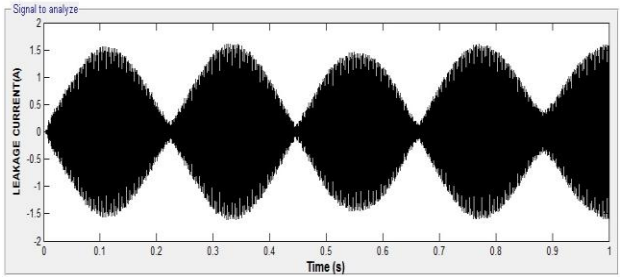

Fig.6 (b).H5 topology leakage current

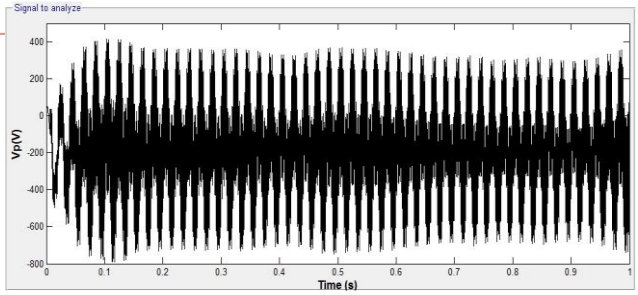

Fig.6 (c).H6 topology parasitic voltage

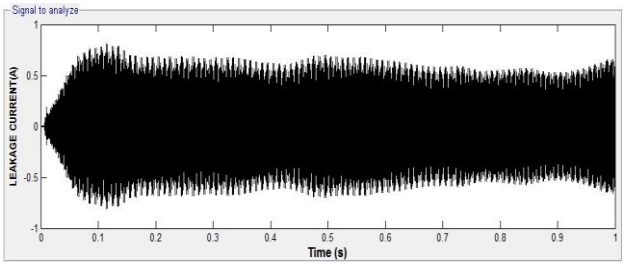

Fig.6 (d).H6 topology leakage current

In view of performance parameters such as leakage current and parasitic voltage, Fig.6 shows that the H5 &H6 topologies are suffered from leakage currents of 1.1100A&0.4459A respectively. As per the literature 1A leakage current is harmful to the system. Even the leakage current of H6 topology is 0.4459A is also need to be reduced for the better performance. Parasitic voltage (V_p) of H5 and H6 topologies are 608.7V and 334.2V respectively. The parasitic capacitor voltage must be equal to the midpoint voltage V_m, otherwise leakage current enhanced rapidly. In proposed system V_m=190V, so that parasitic voltage is also must be 190V. But it was not happen here. That is why it go for closed loop operation. H6 topology has been good benefits than H5 topology. So that H6 topology forward to closed loop operation. In the next section is discussed performance of closed loop operation.

TABLE V. OUTPUT RESULTS OF BOTH TOPOLOGIES

	Inverter Output Voltage[V_o]		Grid Voltage[V_g]			
Topology	***Fundamental***	***%THD***	***Fundamental***	***%THD***	***V_p(V)***	***i_L***(A)
H_5	333.1	32.99	328.4	1.00	608	1.110
H_6	329.9	33.59	328.5	0.98	334	0.445

V. CLOSED LOOP OPERATION

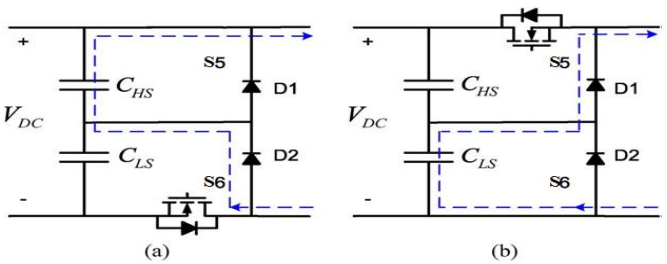

Fig.7. S5 and S6 configurations providing the same voltage V_{MP} to the full bridge rails. In (a), the HS capacitor is discharging, and in (b), the LS capacitor is discharging

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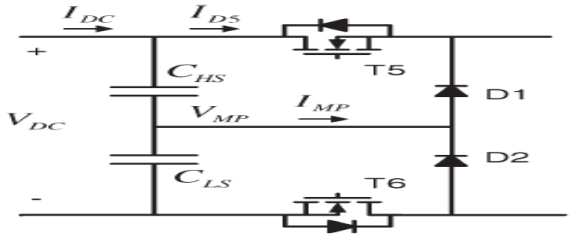

Fig.8. DC capacitor circuit employed for the analytical analysis of the Voltage Balancing.

In ideal (symmetrical) conditions, the theoretical positive and negative voltage levels are present at the output of the power converter for the same time intervals, and no midpoint voltage drift arises. On the contrary, in presence of any asymmetry, the midpoint voltage can drift. The key point for the balancing control of the midpoint voltage is removing the unique correspondence of output voltage levels $+V_{MP}$ and $-V_{MP}$ with the discharging of C_{LS} and C_{HS}, respectively. As a matter of fact, it is possible to provide to the full-bridge output the $+V_{MP}$ or the $-V_{MP}$ voltage through two different configurations. Fig.7 shows the two configurations that provide the voltage level V_{MP} by discharging either C_{HS} [see Fig.7.1 (a)] or C_{LS} [see Fig.7.1 (b)].In addition, in this figure, the controlled power switches that are ON during the whole PWM period are substituted by a solid line.

A suitable determination of the utilization times of the two configurations is able to balance the charge of the two capacitors, as it will be detailed in the following description. In Fig.8, the dc side of the power converter, highlighting the signal of interest, i.e., the dc supply current I_{dc}, the drain current of the transistor S5 is I_{D5}, the midpoint current is I_{MP}, and midpoint voltage is V_{MP}, have shown.

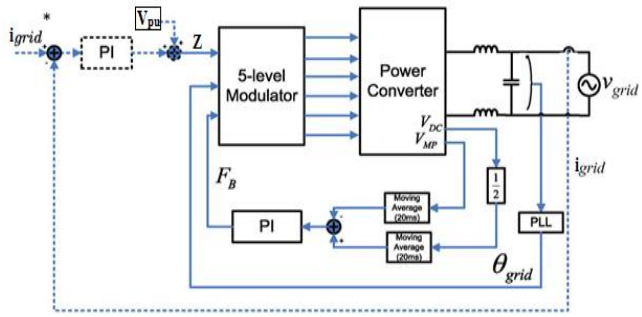

Fig.9. Block scheme of the balancing control of the midpoint voltage

The block scheme of the MVC is shown in Fig.9. The capacitors swap for the midpoint voltage regulation relies on the balancing factor *FB*, which is provided by a proportional integral (PI) regulator. The input of the PI regulator is the difference between the moving averages ($T_{average} = T_{grid\_voltage}$)of V_{MP} and $V_{dc}/2$. The dotted part in Fig. 9 shows a simple closed-loop control (PI + feed forward) of the injected grid current I_{grid} used for simulation and experimental results. In order to fix V_{MP}, the five-level modulator works in this way: the balancing factor *FB* is compared with θ_{grid} (see Fig. 10), and the V_{MP} voltage is provided to the full-bridge rails from the capacitor C_{LS} or C_{HS} through the simple rule shown in below

$\theta_{grid} \geqslant FB \rightarrow C_{LS}$, provides V_{MP}
$\theta_{grid} < FB \rightarrow C_{HS}$, provides V_{MP}.

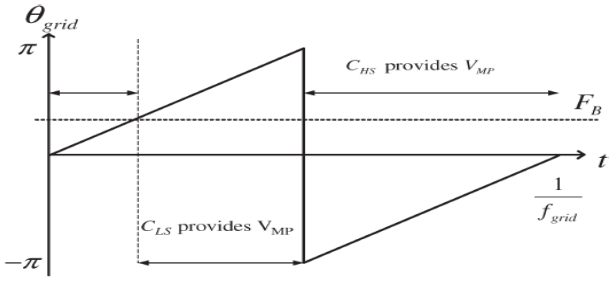

Fig.10. MVC working in case of a positive *FB*

In symmetric conditions, *FB* = 0, the V_{MP} voltage is provided by the low-side capacitor C_{LS} during the whole positive semi-period and by the high-side capacitor C_{HS} during the whole negative semi-period. If an asymmetry arises and, for example, V_{MP} tends toward a lower value, the proposed MVC will use for a longer time interval C_{HS} to provide V_{MP} to the full-bridge rails. In this case the MVC will impose a positive *FB*.

VI. SIMULATION RESULTS AND DISCUSSION

The proposed five level solution was simulated using the MATLAB software, in the fig.9, the simulation parameters wereV_{dc}=317V,V_g=230√2sin(2π50t),L_f=1000μH, C_{HS}=C_{LS}=2mF, ,C_f=2 μF and R_f=0.5Ω. A grid impedance Z_{grid}=(jω50μH+0.4) Ω have been considered

TABLE VI. OUTPUT RESULTS OF H6 TOPOLOGY IN CLOSED LOOP CONFIGURATION

Inverter Output Voltage[V_o]		**Grid Voltage[V_g]**				
Fundamental	***%THD***	***Fundamental***	***%THD***	***V_p(V)***	***i_L(A)***	***V_{mp}(V)***
328.8	17.91	328	0.75	-160.5	0.0468	160.5

The table VI shows the effectiveness of the closed loop configuration of proposed topology. The voltage supplied by solar is around 321.0V.Asspecialy the present leakage current (0.04682A) and %THD (17.91%) had very low values as compared with open loop configuration of the proposed topology. In solar applications parasitic capacitor is formed in between the ground and PV panel. The voltage across the parasitic capacitor is same as the midpoint voltage for getting stability of the whole system. The power converter control, formed by the midpoint voltage control and current control, was the same with that shown in the block scheme in fig.9. The sinusoidal voltage have obtained by the filter and in this project, it assumed the grid current as 6.12A_{RMS}.The all required simulation results with their FFT analysis wave forms are shown below.

Closed loop Simulation results of H6 topology:

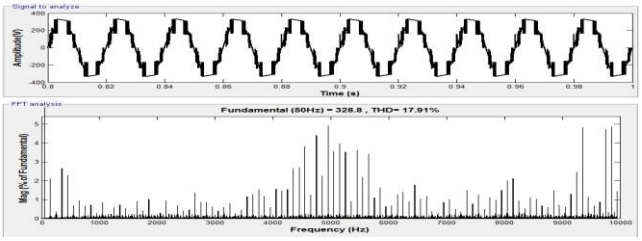

Fig11a: The H6 converter output voltage with FFT analysis

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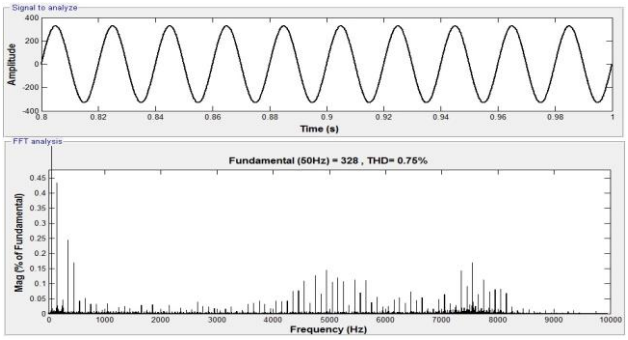

Fig.11(b): the grid injected voltage with FFT analysis

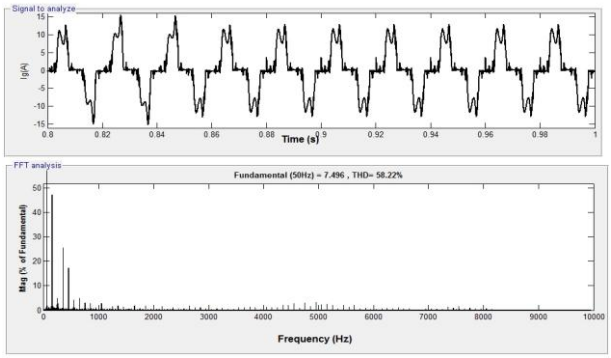

Fig11.(c).grid injected current

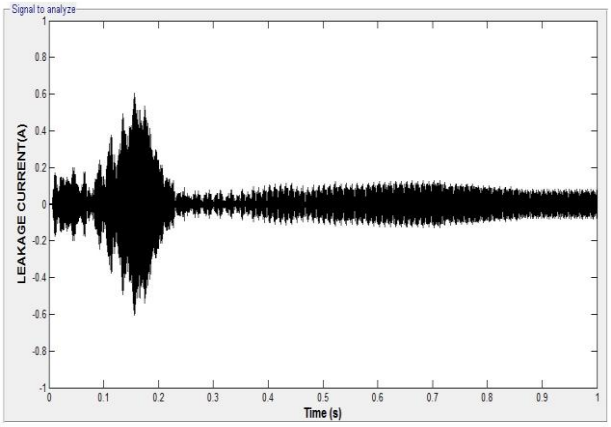

Fig.11 (d) Leakage current

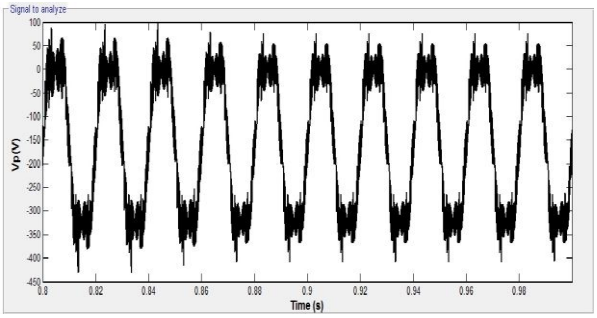

Fig.11(e).parasitic capacitor voltage

VII. CONCLUSION

This paper has dealt with a novel five-level solution for single-phase grid-connected converters. The PWM strategy was chosen in order to obtain the minimum number of commutations to maximize efficiency. The converter topology uses the midpoint voltage of the dc link to provide two more output voltage levels. The balancing of the midpoint voltage was taken into account, and suitable control that was able to compensate for the unavoidable system asymmetries was developed.

The proposed solution was compared with the state of the art of two five-level topologies in terms of %THD, leakage current and parasitic effect. The comparison highlighted that the proposed solution is one of the simplest five-level topologies with power losses in line with the state of the art. As a matter of fact, the PWM strategy developed allows the use of MOSFETs as active devices, making it possible to reduce the conduction power losses. Moreover, an effective balancing control (i.e., MVC) was implemented. It is important to note that the five level output voltage is guaranteed only with a unity power factor operations; otherwise, the converter can output only three voltage levels, thus increasing THD and switching loss. Simulations results showed the feasibility of the proposed converter architecture and the ability of the MVC to compensate for system asymmetries. This paper can extend for practical implementation in the laboratory.

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